

<p><i>Personal</i></p>	<p><i>Date of birth:</i> 15 / 07 / 1976</p> <p><i>Place of birth:</i> Jerusalem, Israel</p> <p><i>Marital status:</i> Married</p> <p><i>Web site:</i> <a href="http://www.cs.huji.ac.il/~etsman">http://www.cs.huji.ac.il/~etsman</a></p> <p><i>Email:</i> <a href="mailto:yoav.etsion@bsc.es">yoav.etsion@bsc.es</a></p> <p><i>Home phone:</i> +34 93 252 1537</p> <p><i>Mobile phone:</i> +34 617 702 967</p> <p><i>Home address:</i> Pg. Senillosa 5, 08034 Barcelona, Spain</p>
<p><i>Current Position</i></p>	<p><i>Affiliation:</i> Barcelona Supercomputing Center (BSC)</p> <p><i>Title:</i> Senior Researcher</p> <p><i>Office address:</i> c/ Jordi Girona 29, 08034 Barcelona, Spain</p> <p><i>Office phone:</i> +34 93 413 7735</p>
<p><i>Research Interests</i></p>	<p><i>Computer Architecture, Operating Systems and Runtime Systems, Parallel Systems, Parallel Programming Models, High-Performance Computing.</i></p>
<p><i>Higher Education</i></p>	<p><b>2008 - 2011</b> <b>Post-doctoral fellowship</b>, Barcelona Supercomputing Center, Host: Prof. Alex Ramirez</p> <p><b>2003 - 2009</b> <b>Ph.D.</b> Computer Science, <i>Hebrew University</i> (Awarded: 9/2009). Thesis title: "<b>The Skewed Distribution of Working Sets: Leveraging Randomness for Cache Design</b>", Advisor: Prof. Dror G. Feitelson.</p> <p><b>1998 - 2002</b> <b>M.Sc.</b> Computer Science (<i>Magna Cum-Laude</i>), <i>Hebrew University</i>, Thesis title: "<b>Scheduling of Interactive Processes: How Can I Play a DVD and Compile Linux at the Same Time</b>". Advisor: Prof. Dror G. Feitelson.</p> <p><b>1995 - 1998</b> <b>B.Sc.</b> Computer Science, <i>Hebrew University</i>.</p>
<p><i>Academic Positions</i></p>	<p><b>2008 -</b> <b>Barcelona Supercomputing Center (BSC-CNS)</b> Senior Researcher.</p> <p><b>2003 - 2008</b> <b>Hebrew University, School of Computer Science &amp; Eng.</b> Teaching assistant.</p> <p><b>2000 - 2003</b> <b>Hadassah College of Technology, Computer Science Dept.</b> Lecturer.</p>

<p><i>Teaching Experience</i></p>	<p><b>2003 – 2008 Hebrew University</b> Course: <i>Introduction to Computer Science</i> (Teaching Assistant)</p> <p><b>2000 – 2003 Hadassah College of Technology</b> Course: <i>Advanced Operating Systems</i> [2002,2003] Course: <i>Operating Systems Project</i> [2000,2001]</p>
<p><i>Professional Societies</i></p>	<p><b>ACM</b> (since 2001), <b>IEEE</b> (since 2002), <b>USENIX</b> (intermittent since 2001)</p>
<p><i>Professional Activities</i></p>	<p>Conference Program Committees: <b>HIPC'10, IPDPS'11</b></p> <p>Workshop Program Committees: <b>PMEA'10, CAOS'10</b></p> <p>Organizing Committee member: <b>PACT'09</b> (Workshops Chair)</p> <p>Workshop Co-Organizers: <b>FASSP'11</b></p>
<p><i>Honors and Awards</i></p>	<p><b>2008-2011 Juan de la Cierva Postdoctoral Fellowship Award</b>, The Spanish Ministry of Science and Innovation</p> <p><b>2010 Best Paper Award</b>, A4MMC'10</p> <p><b>2009 Best Student Paper Award</b>, SMTPS'09</p> <p><b>2006 Intel-dean prize</b> for outstanding PhD student</p> <p><b>2001 USENIX Student Research Grant.</b></p>
<p><i>Research Grants</i></p>	<p><b>2010 – 2014</b> European Commission FP7 IST (FET Proactive initiative), <b>“TERAFLUX: Exploiting Dataflow Parallelism in Teradevice Computing”</b>, Univ. of Sienna, BSC, CAPS Enterprise, HP Labs Spain, INRIA, Microsoft Israel, THALES, Univ. of Augsburg, Univ. of Cyprus, Univ. of Manchester. Project budget 5.7 million EU (844,000EU for BSC)</p> <p>Role: <b>Associate Researcher</b> Co-author of research proposal and responsible for all computer architecture research conducted at BSC for the project.</p>
<p><i>Publications:</i> <b>Book Chapters</b></p>	<p>D. G. Feitelson, A. Batat, G. Benhanokh, D. Er-EI, Y. Etsion, A. Kavas, T. Klainer, U. Lublin, and M. A. Volovic, <b>“The ParPar System: A Software MPP”</b>, In <i>High Performance Cluster Computing, Vol. 1: Architectures and Systems</i>, Rajkumar Buyya (Ed.), Prentice-Hall, pp. 754-770, 1999</p>
<p><i>Publications:</i> <b>Journal Articles</b></p>	<p>Yoav Etsion and Dror G. Feitelson, <b>“Exploiting Core Working Sets to Filter the L1 Cache with Random Sampling”</b>, Submitted to IEEE Trans. On Computers (TC).</p> <p>Dror Feitelson, Tokunbo O. S. Adeshiyani, Daniel Balasubramanian, Yoav Etsion, Gabor Madl, Esteban P. Osses, Sameer Singh, Karlkim Suwanmongkol, Charlie Xie, and Stephen R. Schach <b>“Fine-Grain Analysis of Common Coupling and its Application to a Linux Case Study”</b>. In <i>Journal of Systems and Software (JSS)</i>, <b>80(8)</b>, pp. 1239-1255, Aug. 2007.</p>

	<p>Dan Tsafir, Yoav Etsion and Dror G. Feitelson, "<b>Backfilling Using System-Generated Predictions Rather than User Runtime Estimates</b>", In <i>IEEE Transactions on Parallel and Distributed Systems (TPDS)</i>, <b>18(6)</b>, pp. 789-803, Jun. 2007.</p> <p>Yoav Etsion and Dror G. Feitelson, "<b>Probabilistic Prediction of Temporal Locality</b>", In <i>IEEE Computer Architecture Letters (CAL)</i>, <b>6(1)</b>, pp. 17-20, May 2007.</p> <p>Yoav Etsion, Dan Tsafir and Dror G. Feitelson, "<b>Process Prioritization Using Output Production: Scheduling for Multimedia</b>". In <i>ACM Trans. on Multimedia Computing, Communications, and Applications. (TOMCCAP)</i>, <b>2(4)</b>, pp. 318-342, Nov. 2006.</p>
<p><i>Publications:</i> <b>Conference Papers</b></p>	<p>Carlos Villavieja, Vasilis Karakostas, Lluís Vilanova, Yoav Etsion, Alex Ramirez, Avi Mendelson, Nacho Navarro, Adrian Cristal, and Osman Unsal, "<b>DiDi: Mitigating The Performance Impact of TLB Shootdowns Using A Shared TLB Directory</b>". In <i>20<sup>th</sup> Intl. Conf. on Parallel Architectures and Compilation Techniques (PACT)</i>, Oct. 2011. (to appear)</p> <p>Carlos Villavieja, Yoav Etsion, Alex Ramirez, and Nacho Navarro, "<b>FELI: HW/SW support for On-Chip Distributed Shared Memory in Multicores</b>". In <i>Euro-Par</i>, Aug. 2011. (to appear)</p> <p>Alejandro Rico, Alex Duran, Felipe Cabarcas, Alex Ramirez, Yoav Etsion, and Mateo Valero. "<b>Trace-driven Simulation of Multithreaded Applications</b>", In <i>IEEE Intl. Symp. Performance Analysis of Systems and Software (ISPASS)</i>, Apr. 2011.</p> <p>Yoav Etsion, Felipe Cabarcas, Alejandro Rico, Alex Ramirez, Rosa M. Badia, Eduard Ayguade, Jesus Labarta, and Mateo Valero, "<b>Task Superscalar: An Out-of-Order Task Pipeline</b>". In <i>IEEE/ACM Intl. Symp. on Microarchitecture (MICRO-43)</i>, Dec 2010.</p> <p>Felipe Cabarcas, Alejandro Rico, Yoav Etsion, and Alex Ramirez, "<b>Interleaving Granularity on High Bandwidth Memory Architecture for CMPs</b>", In <i>10<sup>th</sup> Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)</i>, Jul 2010.</p> <p>Yoav Etsion, Alex Ramirez, Rosa M. Badia, Eduard Ayguade, Jesus Labarta, and Mateo Valero, "<b>Task Superscalar: Using Processors as Functional Units</b>". In <i>2<sup>nd</sup> USENIX Workshop on Hot Topics In Parallelism (HotPar)</i>, Jun. 2010.</p> <p>Milan Pavlovic, Yoav Etsion, and Alex Ramirez, "<b>Can Manycores Support the Memory Requirements of Scientific Applications?</b>". In <i>Workshop on Applications for Multi and Many Core Processors (A4MMC)</i>, Jun. 2010 <b>Best Paper Award</b></p> <p>Tal Ben-Nun, Yoav Etsion, and Dror G. Feitelson, "<b>Design and Implementation of a Generic Resource Sharing Virtual Time Dispatcher</b>". In <i>3rd SYSTOR</i>, May 2010.</p> <p>Yoav Etsion, Alex Ramirez, Rosa M. Badia and Jesus Labarta, "<b>Cores as Functional Units: A Task-Based, Out-of-Order, Dataflow Pipeline</b>". In <i>Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)</i>, Jul 2009. (extended abstract).</p>

	<p>Yoav Etsion, Tal Ben-Nun and Dror G. Feitelson, “<b>A Global Scheduling Framework for Virtualization Environments</b>”. In <i>Workshop on System Management Techniques, Processes and Services (SMTPS)</i>, May 2009. <b>Best Student Paper Award</b></p> <p>Yoav Etsion and Dror G. Feitelson, “<b>L1 Cache Filtering Through Random Selection of Memory References</b>”, In 16<sup>th</sup> <i>Intl. Conf. on Parallel Architectures and Compilation Techniques (PACT)</i>, Sep. 2007.</p> <p>Dan Tsafir, Yoav Etsion and Dror G. Feitelson, “<b>Secretly monopolizing the CPU without superuser privileges</b>”, In 16<sup>th</sup> <i>USENIX Security Symposium</i>, Aug. 2007.</p> <p>Yoav Etsion, Dan Tsafir, Scott Kirkpatrick, Dror G. Feitelson, “<b>Fine Grained Kernel Logging with KLogger: Experience and Insights</b>”, In 2<sup>nd</sup> <i>ACM EuroSys</i>, Mar. 2007.</p> <p>Eitan Frachtenberg and Yoav Etsion, “<b>Hardware Parallelism: Are Operating Systems Ready? (Case Studies in Mis-Scheduling)</b>”. In 2<sup>nd</sup> <i>Workshop on the Interactions between Operating Systems and Computer Architecture (WIOSCA)</i>, Jun. 2006.</p> <p>Dan Tsafir, Yoav Etsion and Dror G. Feitelson, “<b>Modeling User Runtime Estimates</b>”. In <i>11th Workshop on Job Scheduling Strategies for Parallel Processing (JSSPP)</i>. D. G. Feitelson, E. Frachtenberg, L. Rudolph, and U. Schwiegelshohn (Eds.), pp. 1-35, Springer-Verlag, 2005. Lecture Notes in Computer Science Vol. 3834</p> <p>Dan Tsafir, Yoav Etsion, Dror G. Feitelson and Scott Kirkpatrick “<b>System Noise, OS Clock Ticks, and Fine-Grained Parallel Applications</b>”. In the 19<sup>th</sup> <i>ACM International Conference on Supercomputing (ICS)</i>, Jun. 2005.</p> <p>Yoav Etsion, Dan Tsafir, and Dror G. Feitelson, “<b>Desktop Scheduling: How Can We Know What the User Wants?</b>”, In <i>14th ACM International Workshop on Network and Operating Systems Support for Digital Audio and Video (NOSSDAV)</i>, Jun .2004.</p> <p>Yoav Etsion, Dan Tsafir, and Dror G. Feitelson, “<b>Effects of clock resolution on the scheduling of interactive and soft real-time processes</b>”. In the Intl. Conf. On Measurement &amp; Modeling of Computer Systems (SIGMETRICS), Jun. 2003.</p> <p>Yoav Etsion and Dror G. Feitelson, “<b>User-Level Communication in a System with Gang Scheduling</b>”, In <i>15th Intl. Parallel and Distributed Processing Symp. (IPDPS)</i>, Apr. 2001.</p>
<p><i>Publications:</i></p> <p><b>Technical Reports</b></p>	<p>Yoav Etsion and Dror G. Feitelson, “<b>Core Working Sets: Concept, Identification, and Use</b>”, Technical Report 2008-64, School of Computer Science and Engineering, The Hebrew University of Jerusalem, Jul. 2008.</p> <p>Tal Ben-Nun, Yoav Etsion and Dror G. Feitelson “<b>The Klogger Networking Schema</b>”, Technical Report 2008-1, School of Computer Science and Engineering, The Hebrew University of Jerusalem, Jan. 2008.</p> <p>Yoav Etsion and Dror G. Feitelson, “<b>Cache Insertion Policies to Reduce Bus Traffic and Cache Conflicts</b>”. Technical Report 2006-4, School of Computer Science and Engineering, The Hebrew University of Jerusalem, Feb. 2006.</p>

	<p>Yoav Etsion and Dan Tsafir, "<b>A Short Survey of Commercial Cluster Batch Schedulers</b>". Technical Report 2005-13, <i>School of Computer Science and Engineering, The Hebrew University of Jerusalem</i>, May 2005.</p> <p>Dan Tsafir, Yoav Etsion, and Dror G. Feitelson, "<b>General Purpose Timing: The Failure of Periodic Timers</b>". Technical Report 2005-6, <i>School of Computer Science and Engineering, The Hebrew University of Jerusalem</i>, Feb. 2005.</p> <p>Yoav Etsion and Dror G. Feitelson, "<b>Time Stamp Counters Library - Measurements with Nano Seconds Resolution</b>", Technical Report 2000-36, <i>School of Computer Science and Engineering, The Hebrew University of Jerusalem</i>, 2000.</p>
<p><i>Patents</i></p>	<p>"<b>System and Method for Backfilling with System-Generated Predictions Rather than User Runtime Estimates</b>", Feb 2006, USPTO Pending Application <i>PCT/IL2006/000199</i>.</p>