

Timing in Sequential circuits –
Stabilization time of a latch

Assume that:
 $t_{hl,1} = t_{lh,1} = t_{hl,2} = t_{lh,2} = 1$ time unit

Timing in Sequential circuits –
Stabilization time of a latch

| Time | R | S | Q _t | Q' _t | Q _{t+1} | Q' _{t+1} |
|------|---|---|----------------|-----------------|------------------|-------------------|
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| | | | | | | |
| | | | | | | |

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Stabilization time of a latch

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|------|---|---|----------------|-----------------|------------------|-------------------|
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 1 | 0 | 1 | 1 | 0 | 1 |
| | | | | | | |
| | | | | | | |

Timing in Sequential circuits –
Stabilization time of a latch

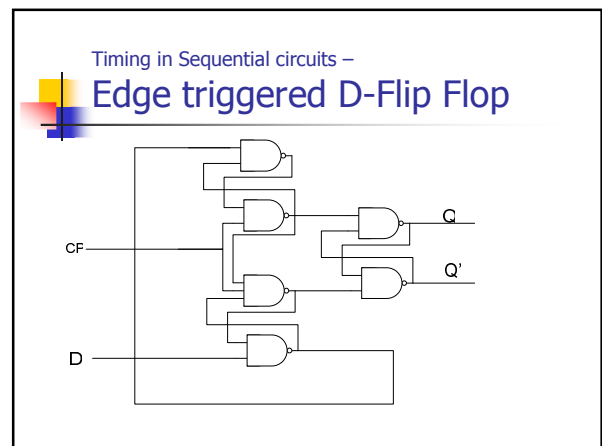
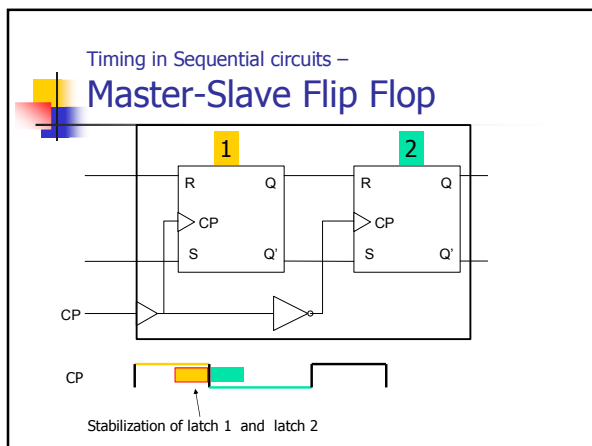
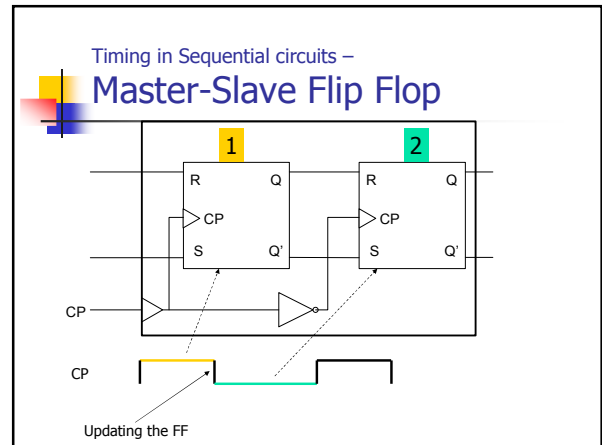
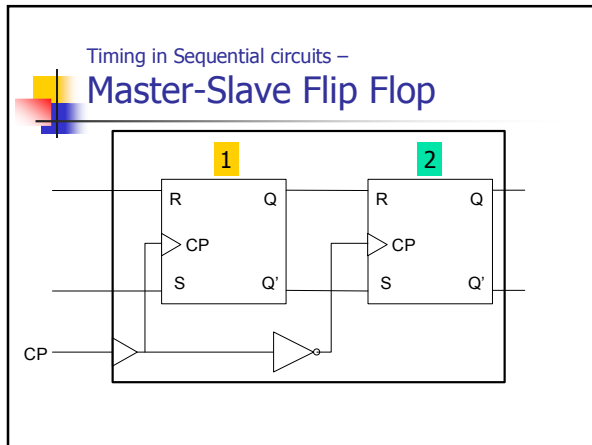
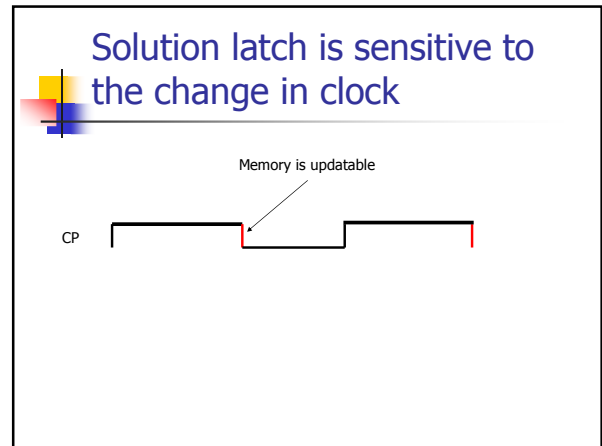
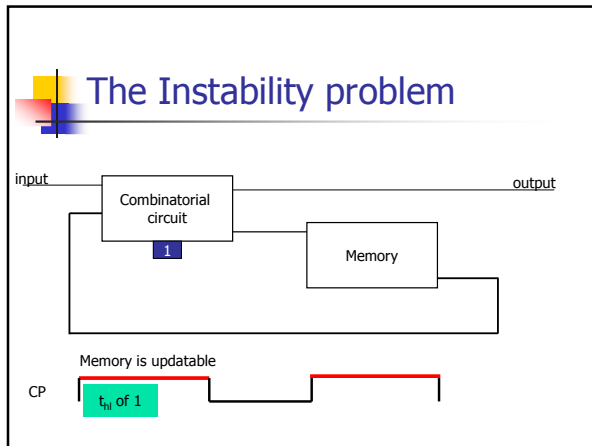
| Time | R | S | Q _t | Q' _t | Q _{t+1} | Q' _{t+1} |
|------|---|---|----------------|-----------------|------------------|-------------------|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 0 | 1 | 1 |
| 3 | 1 | 0 | 0 | 1 | 0 | 1 |
| | | | | | | |
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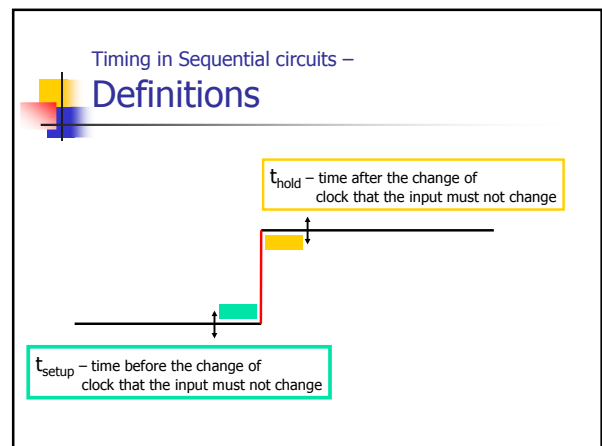
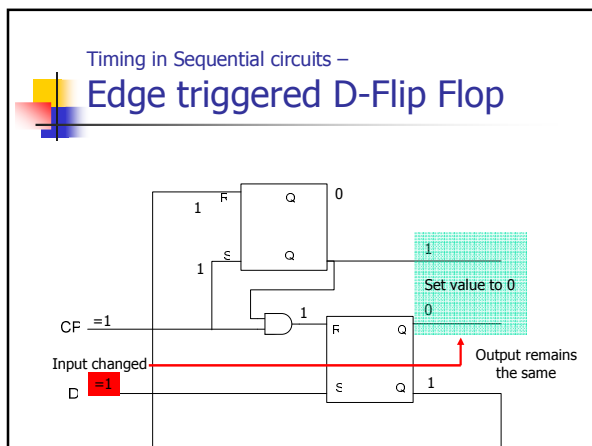
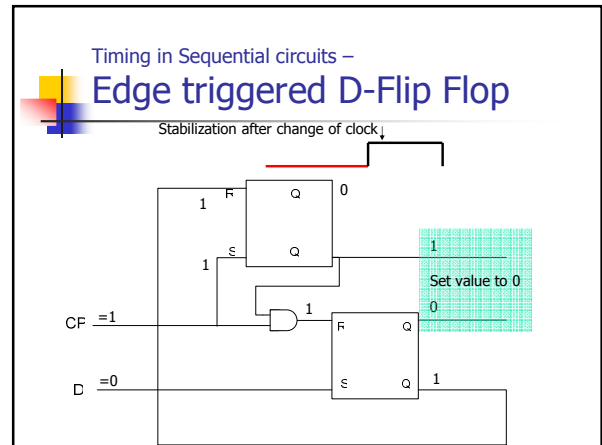
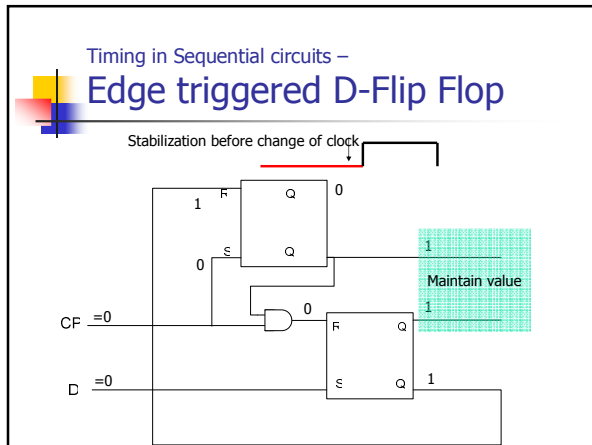
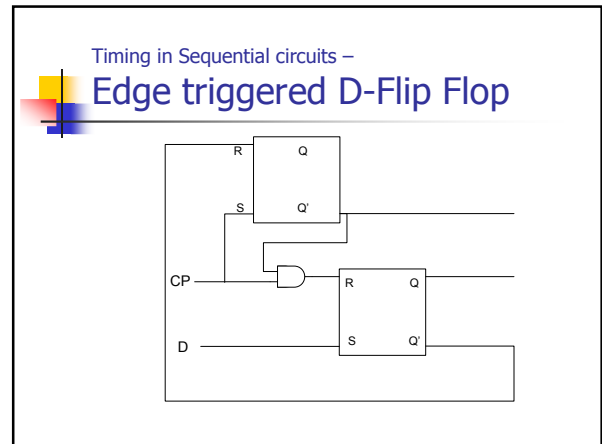
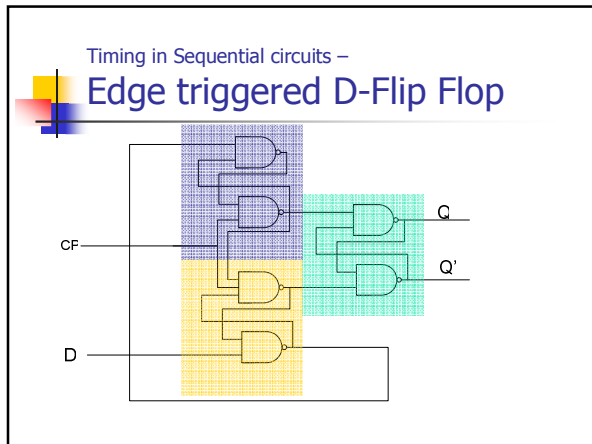
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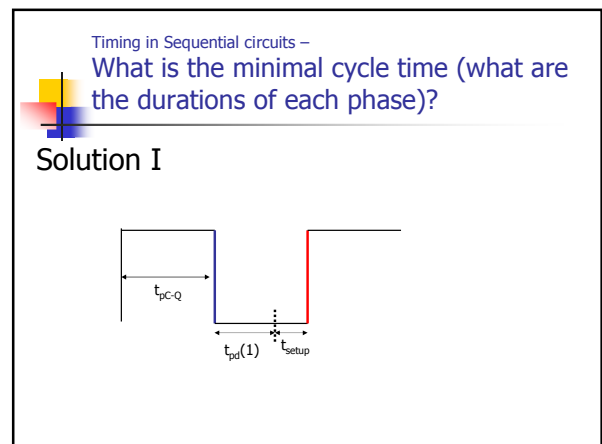
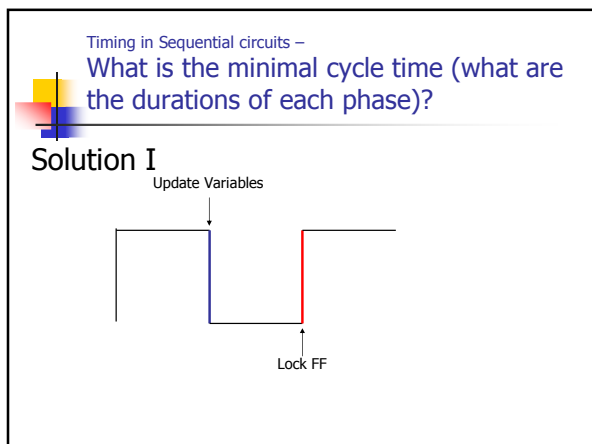
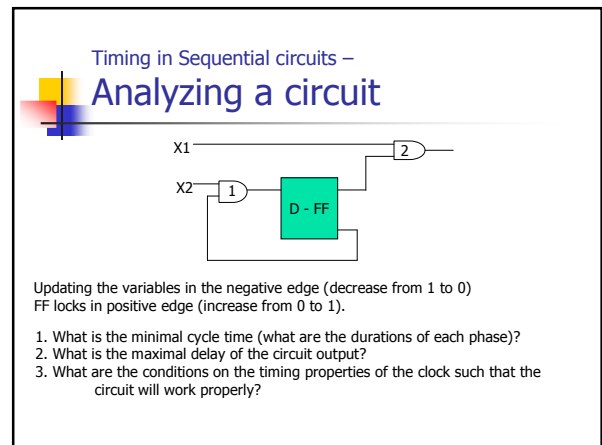
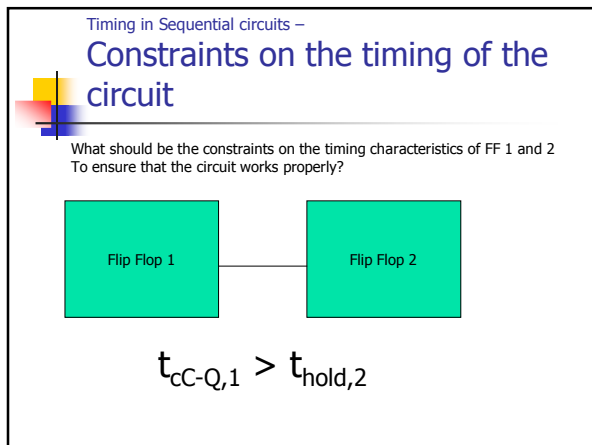
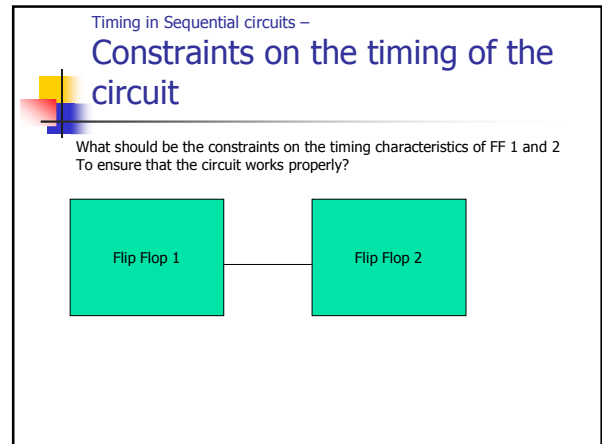
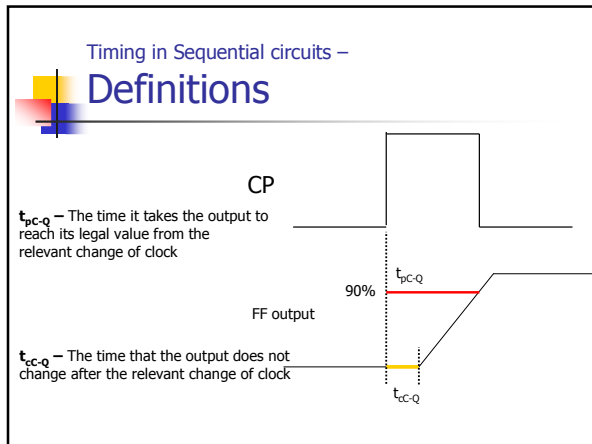
| Time | R | S | Q _t | Q' _t | Q _{t+1} | Q' _{t+1} |
|------|---|---|----------------|-----------------|------------------|-------------------|
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |

It takes time unit for the latch to stabilize

clock controlled latch







Timing in Sequential circuits –
What is the minimal cycle time (what are the durations of each phase)?

Solution II

Timing in Sequential circuits –
What is the maximal delay of the circuit output?

Solution:

$t_{pd} =$

Timing in Sequential circuits –
What is the maximal delay of the circuit output?

Solution:

$t_{pd} = t_{pd}(2)$

The relevant clock change.
 The FF is already updated here

Timing in Sequential circuits –
What are the conditions on the timing properties of the clock such that the circuit will work properly?

Solution:

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What are the conditions on the timing properties of the clock such that the circuit will work properly?

Solution:

$t_{hold} < t_{cd}(1) + t_{cC-Q}$