

Timing and Hazards

Logical levels

Positive Logic

5v = 1

0v = 0

Negative Logic

0v = 1

5v = 0

Noise – basic concepts

Ideal World

Noise – basic concepts

Positive Logic

Ideal World

Real World

Noise – basic concepts

Positive Logic

Real World

Noise – basic concepts

High Value

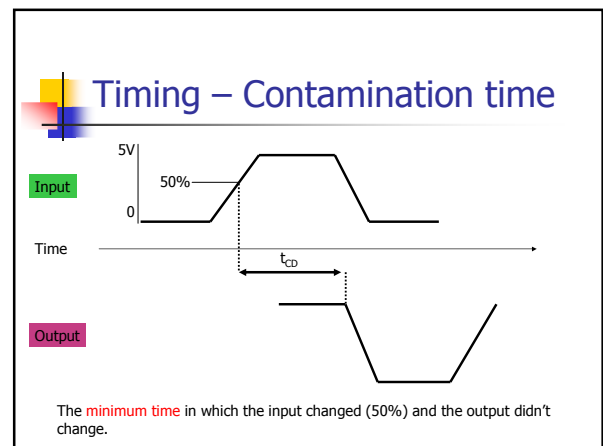
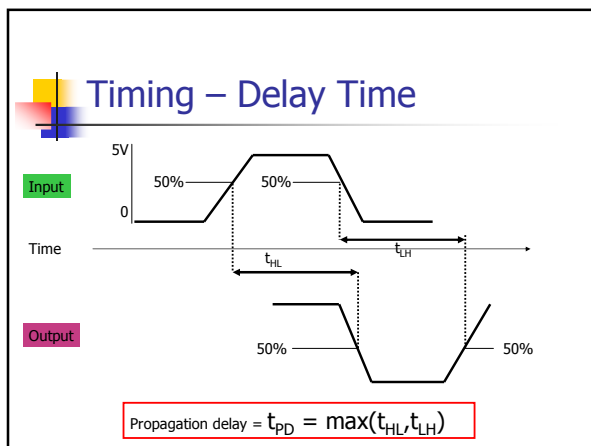
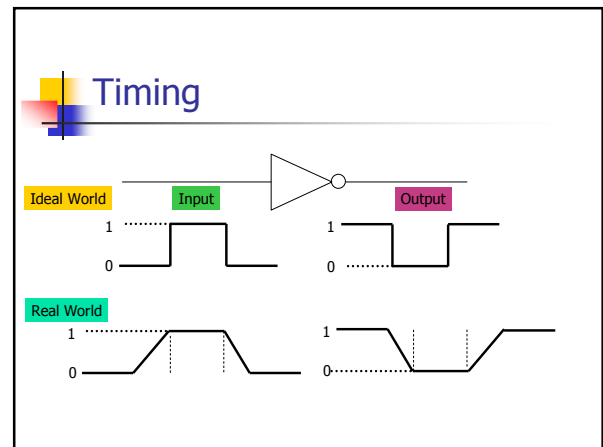
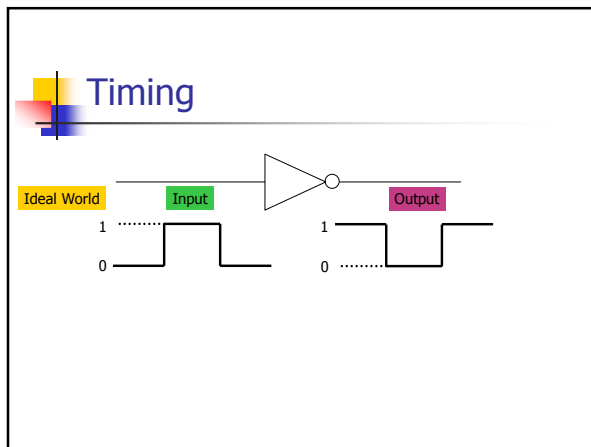
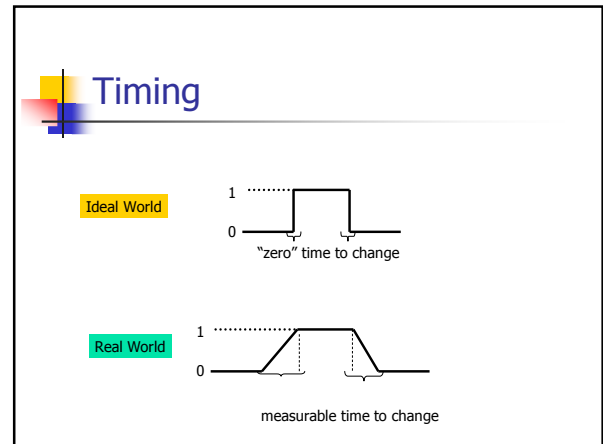
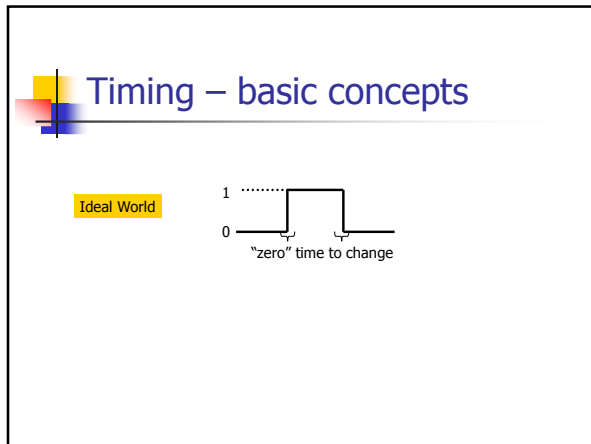
Input Range: 3.5v to 5v

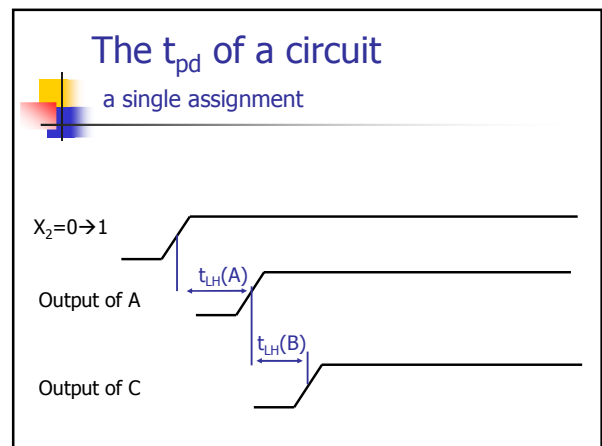
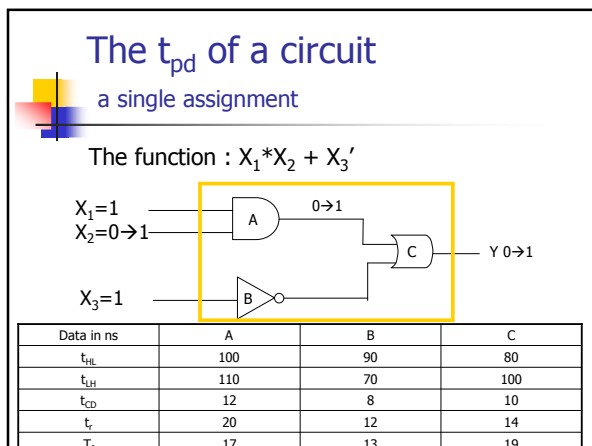
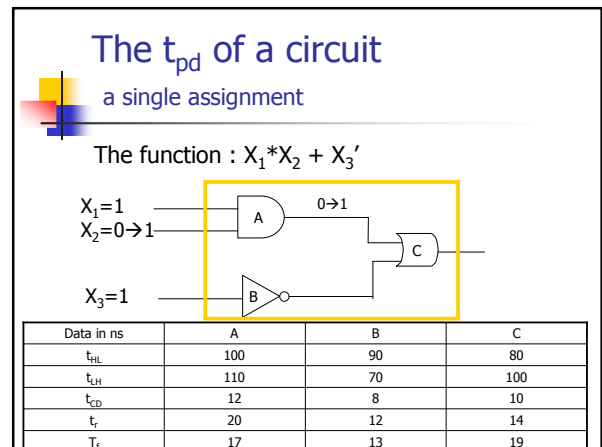
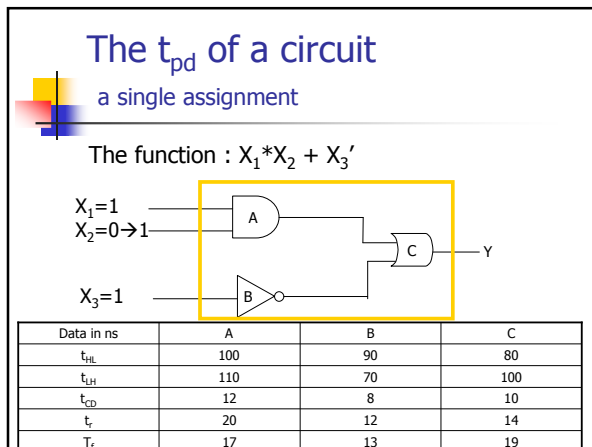
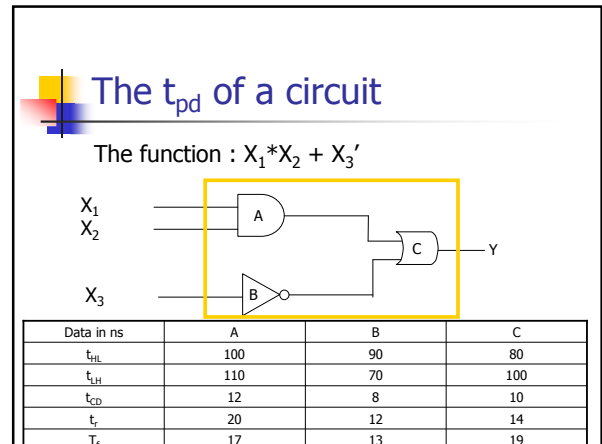
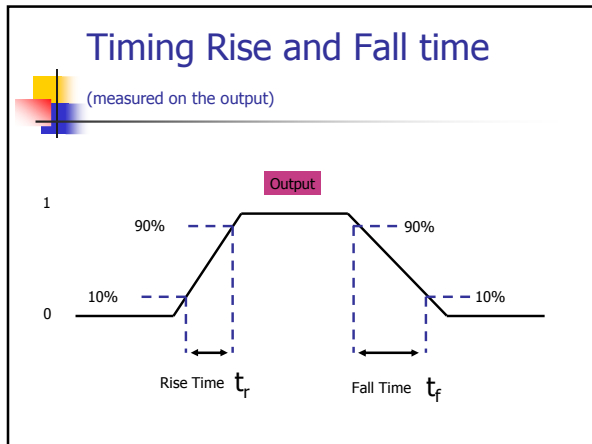
Output Range: 4v to 5v

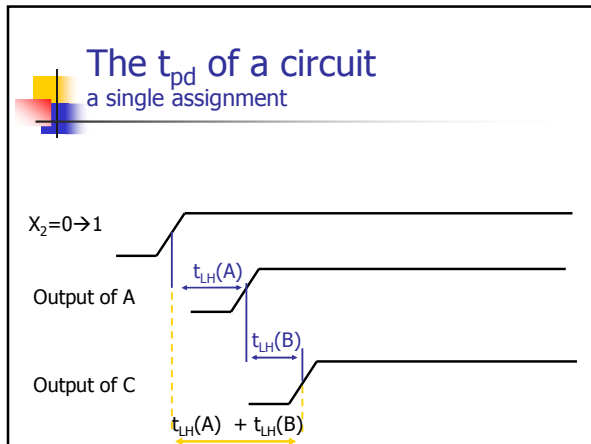
Low Value

Input Range: 0v to 1.5v

Output Range: 0v to 1v

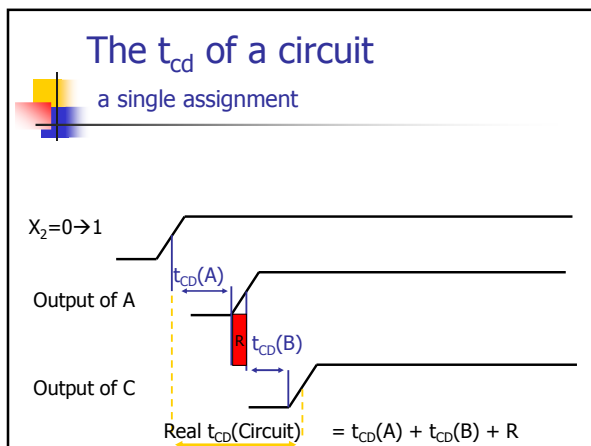
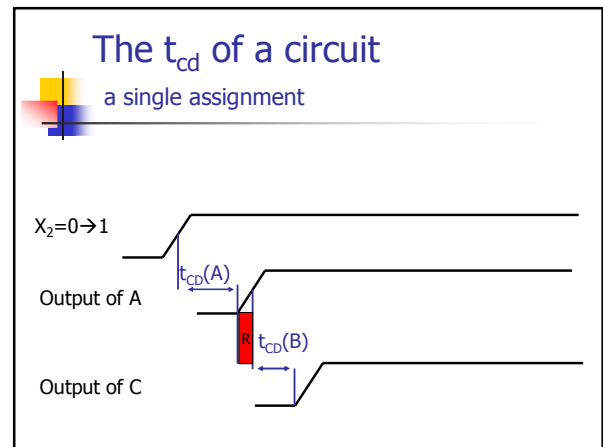
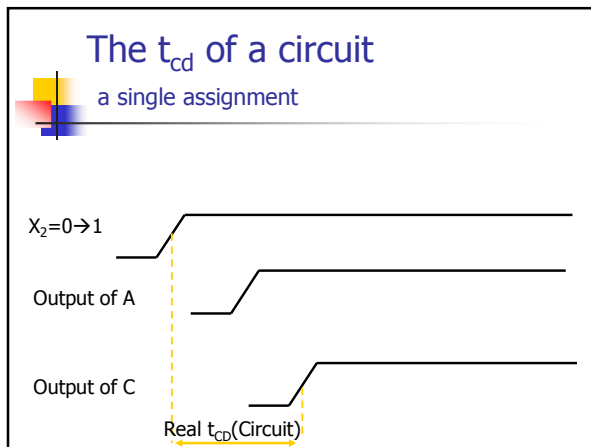






The t_{pd} of a circuit

The t_{pd} of a circuit is the maximal value Over all the possible single assignments



The t_{cd} of a circuit a single assignment

- Since t_{cd} is the **minimum**

$$t_{cd}(\text{Circuit}) = t_{cd}(A) + t_{cd}(B) <$$

$$t_{cd}(A) + t_{cd}(B) + R = \text{Real } t_{cd}(\text{circuit})$$

The t_{CD} of a circuit

The t_{CD} of a circuit is the minimal value
Over all the possible single assignments

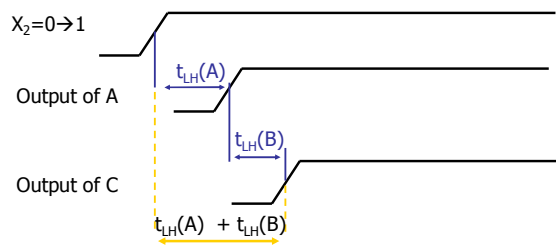
Timing

The minimum time for the output to change

What is the minimal time that the output
will change over a single assignment?

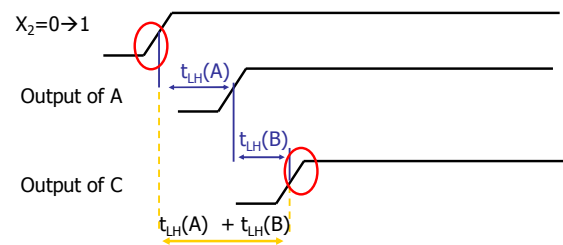
The minimum time for the output to change

a single assignment



The minimum time for the output to change

a single assignment



The minimum time for the output to change

a single assignment

Real Minimum Time =

$$t_{LH}(A) + t_{HL}(A) + \frac{T_r(X_2) + T_r(C)}{2}$$

The minimum time for the output to change

a single assignment

Real Minimum Time =

$$t_{LH}(A) + t_{HL}(A) + \frac{T_r(X_2) + T_r(C)}{2}$$

< $\text{Max}(Tr(X_2), Tr(C))$

The minimum time for the output to change
a single assignment

Estimated Minimum Time =

$$t_{LH}(A) + t_{HL}(A) + \text{Max}(T_r(X2), T_r(C)) >$$

Real Minimum time

Problems in timing

$Y = X2 * X3 + X1 * X2'$

Assume $t_{HL} = t_{LH} > 0$
And equal for all gates

A logic diagram showing three inputs: X1, X2, and X3. X1 is connected to an AND gate (B). X2 is connected to an inverter (A) and an AND gate (C). X3 is connected to AND gate (C). The outputs of gates B and C are connected to an OR gate (D), which produces the output Y.

Problems in timing

$Y = X2 * X3 + X1 * X2'$

The logic diagram from the previous slide with input values: X1=1, X2=1, X3=1. The output Y is 1.

Problems in timing

$Y = X2 * X3 + X1 * X2'$

The logic diagram with the same input values as the previous slide. Intermediate values are shown: the output of gate A is 0, the output of gate B is 0, and the output of gate C is 1. The final output Y is 1.

Change in input – final state

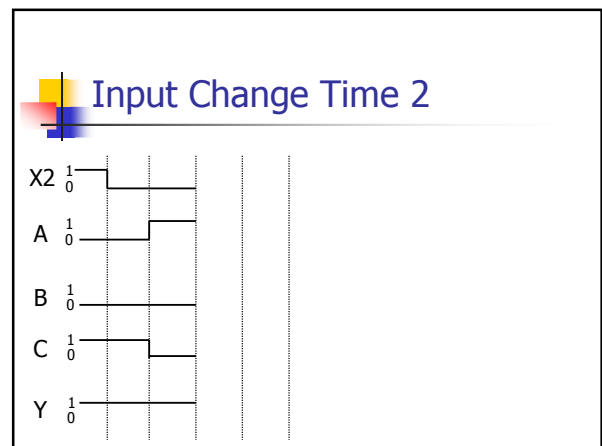
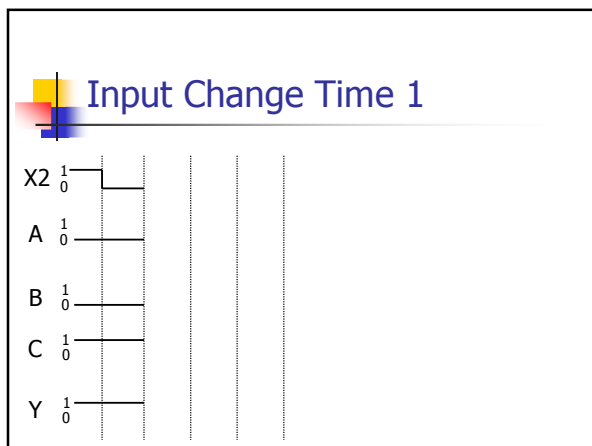
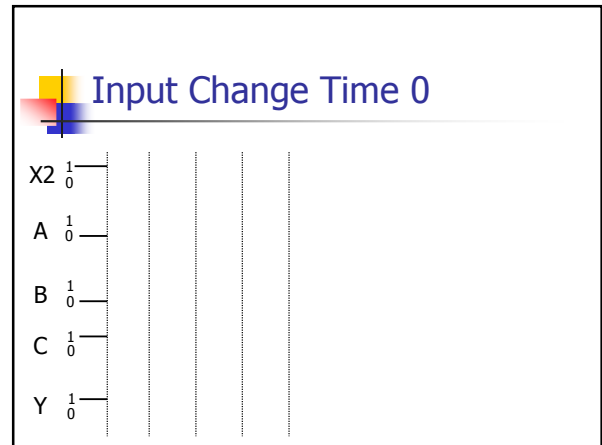
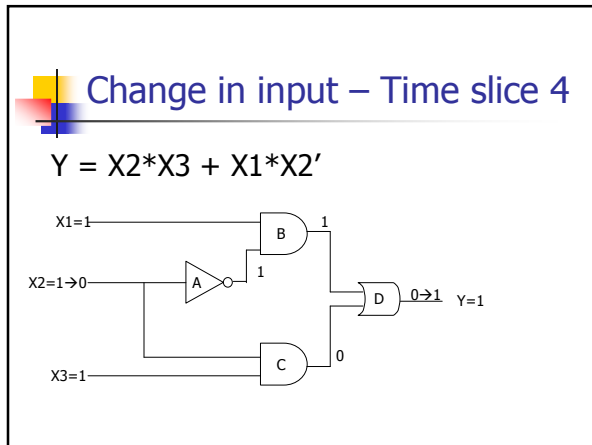
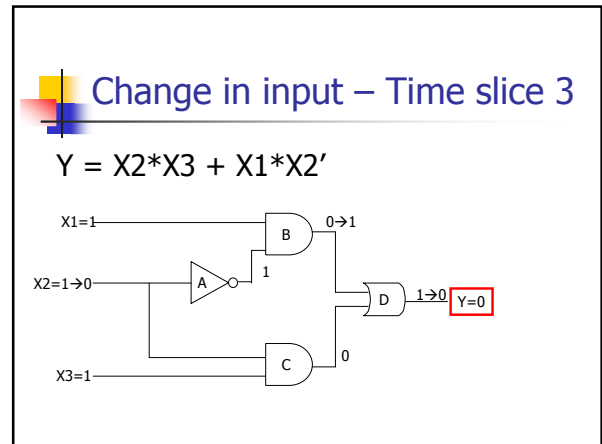
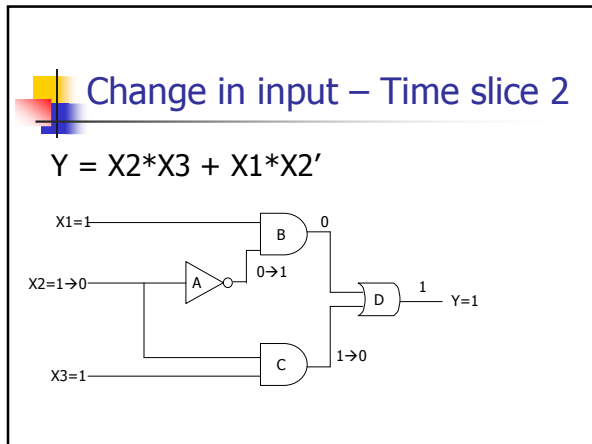
$Y = X2 * X3 + X1 * X2'$

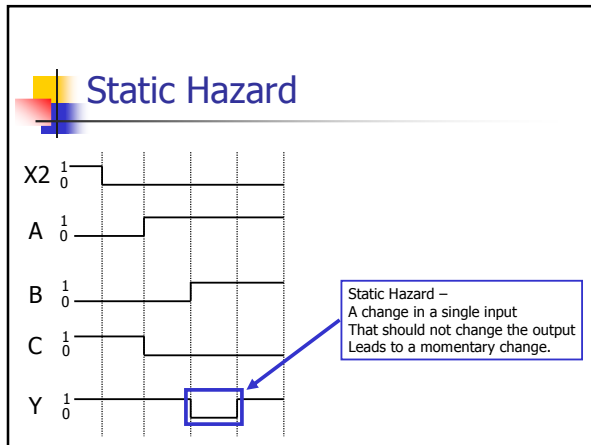
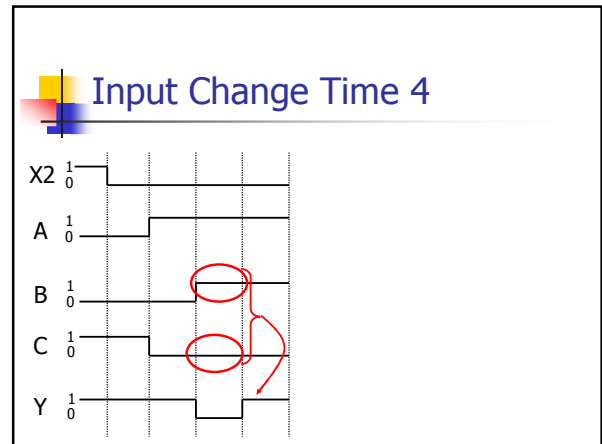
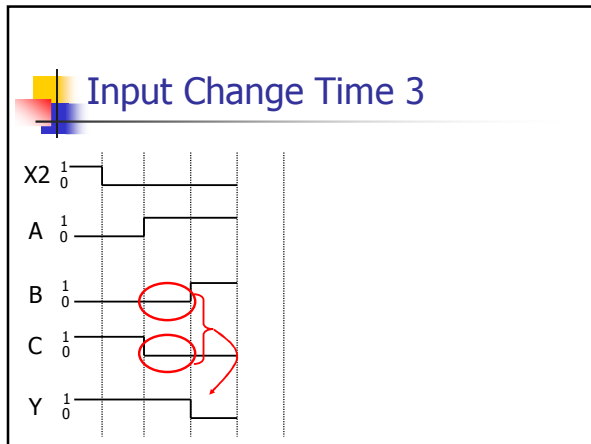
The logic diagram with input values: X1=1, X2=1→0, X3=1. The output Y is 1. A callout box says: "We changed the input But the result remained the same".

Change in input – Time slice 1

$Y = X2 * X3 + X1 * X2'$

The logic diagram with input values: X1=1, X2=1→0, X3=1. The output Y is 1.





Static hazard – another point of view

$x_1 \backslash x_2 x_3$	00	01	11	10
0			1	
1	1	1	1	

Static hazard – another point of view

$x_1 \backslash x_2 x_3$	00	01	11	10
0			1	
1	1	1	1	

Static hazard – another point of view

$x_1 \backslash x_2 x_3$	00	01	11	10
0			1	
1	1	1	1	