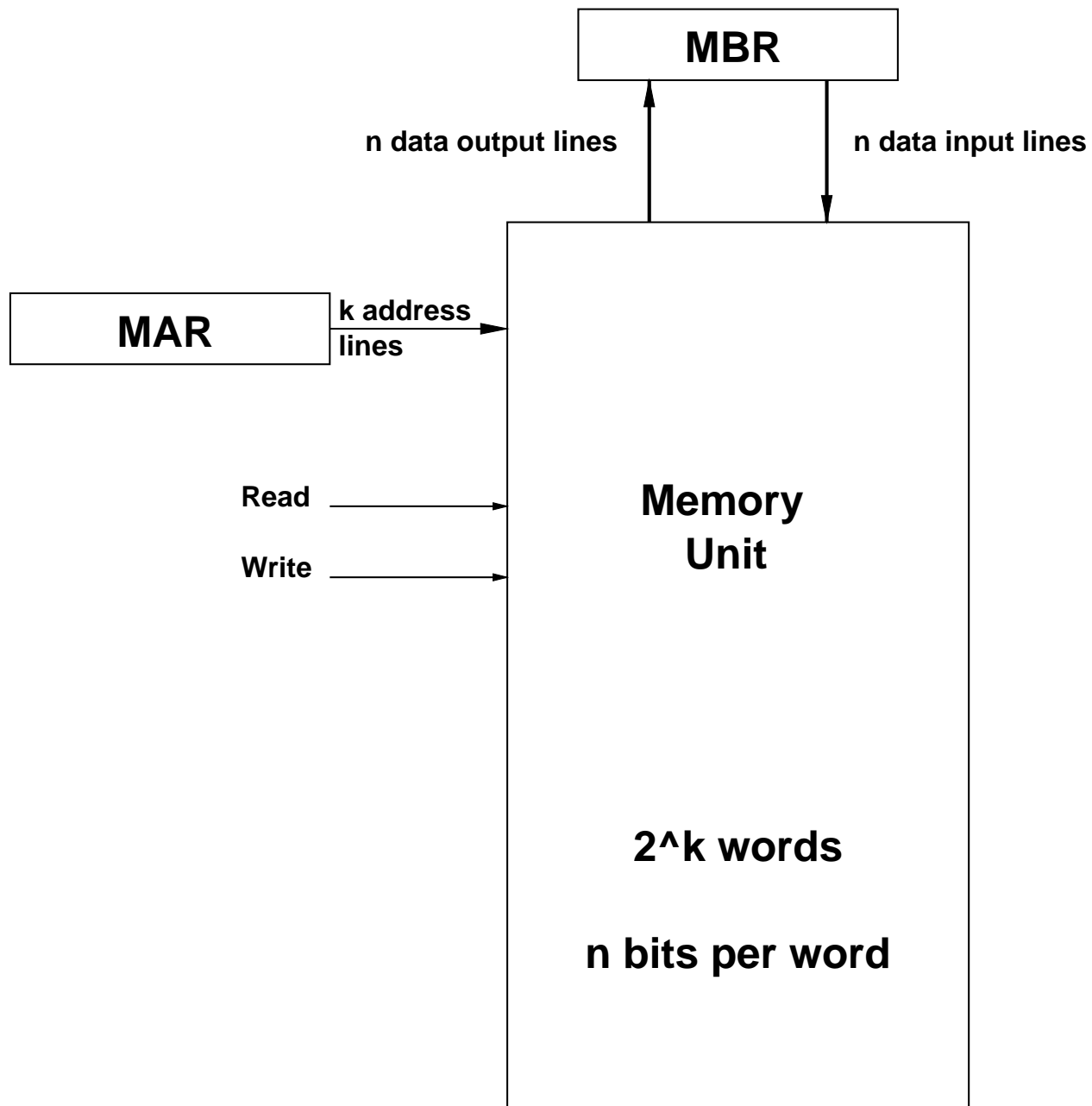
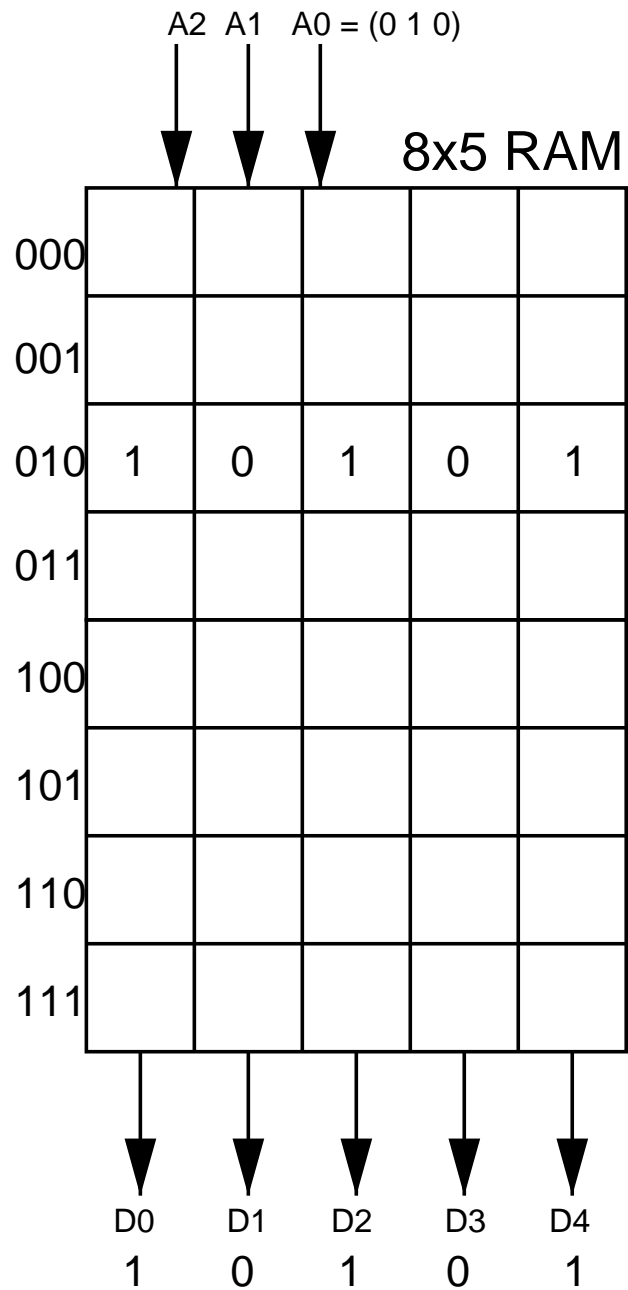


Memory Units

- Store integer and floating point numbers, pointers, ...
- Different types of memory:
Static RAM, Dynamic RAM, ROM
- Static RAM: simple and fast **latches** grouped together
- Memory is accessed through two special registers:
 - **MAR** Memory Address Register
 - **MBR** Memory Buffer Register





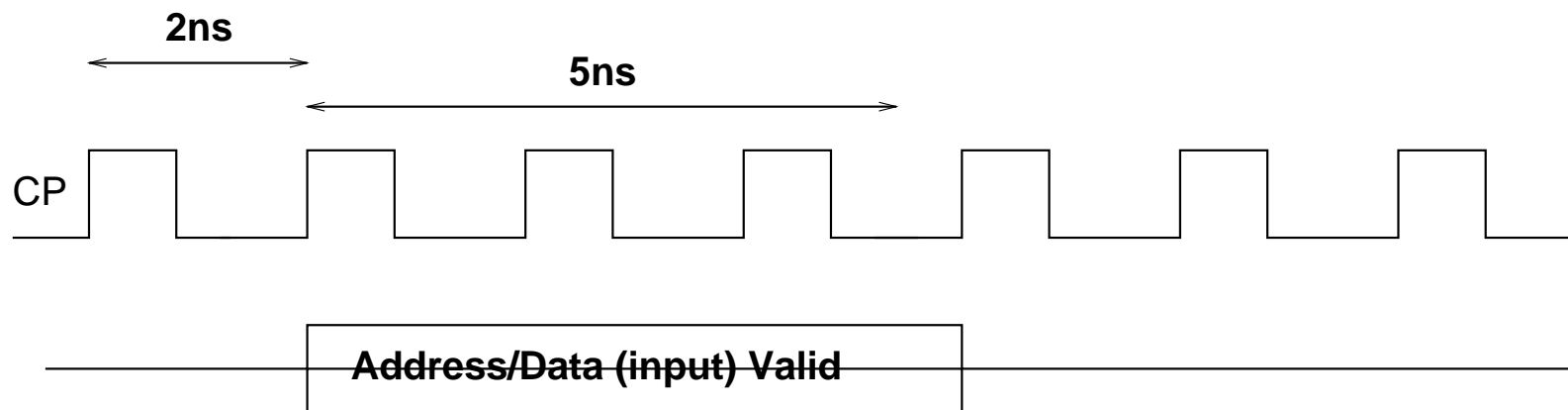
Terminology

- Each entry in a memory unit is called a **word**
- Each word is composed of n bits (width)
- Size of a RAM is the number of words 2^k
- Common widths: Byte (8 bits), Short (16 bits), Int (32 bits)
- The size of a RAM is denoted as $2^k \times n$:
1024 × 16, 128Mb = $2^{27} \times 8$

Write Cycle

1. Move the *address* of the word to be written to MAR
 2. Move the *content* of the word to be written to MBR
 3. Turn the *write* input line on
- ★ Steps 1 and 2 can be done in parallel

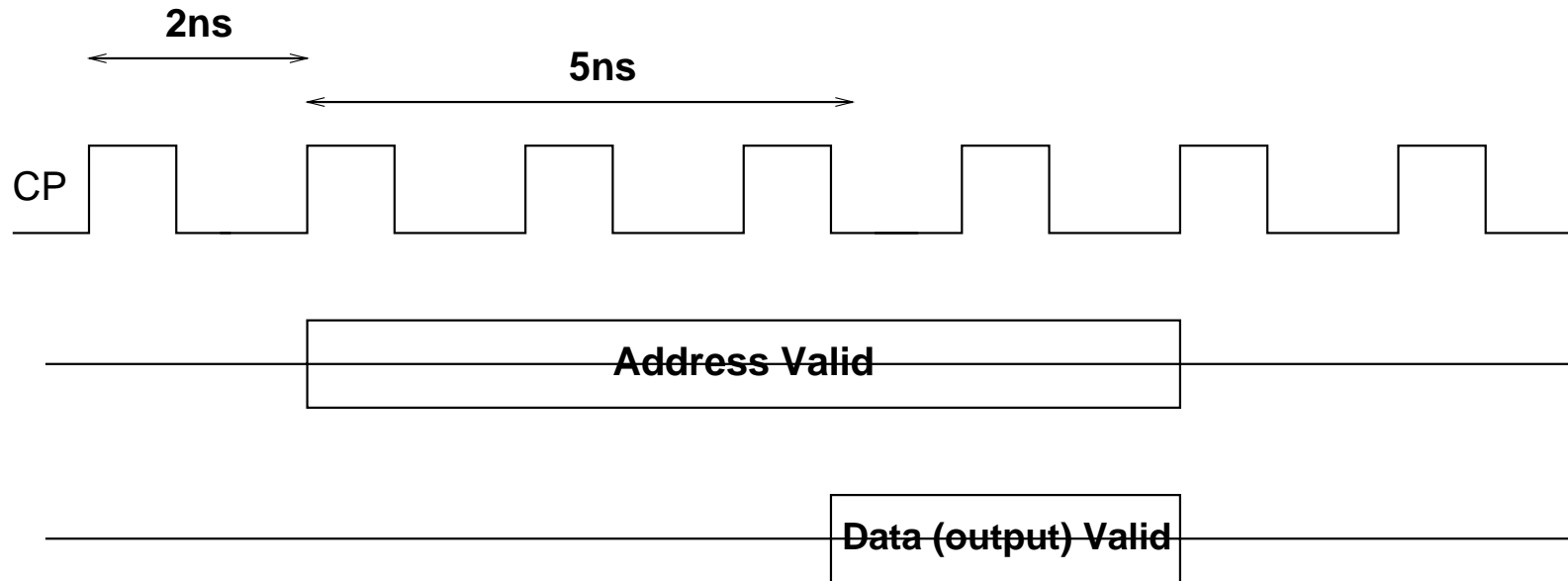
Write Cycle



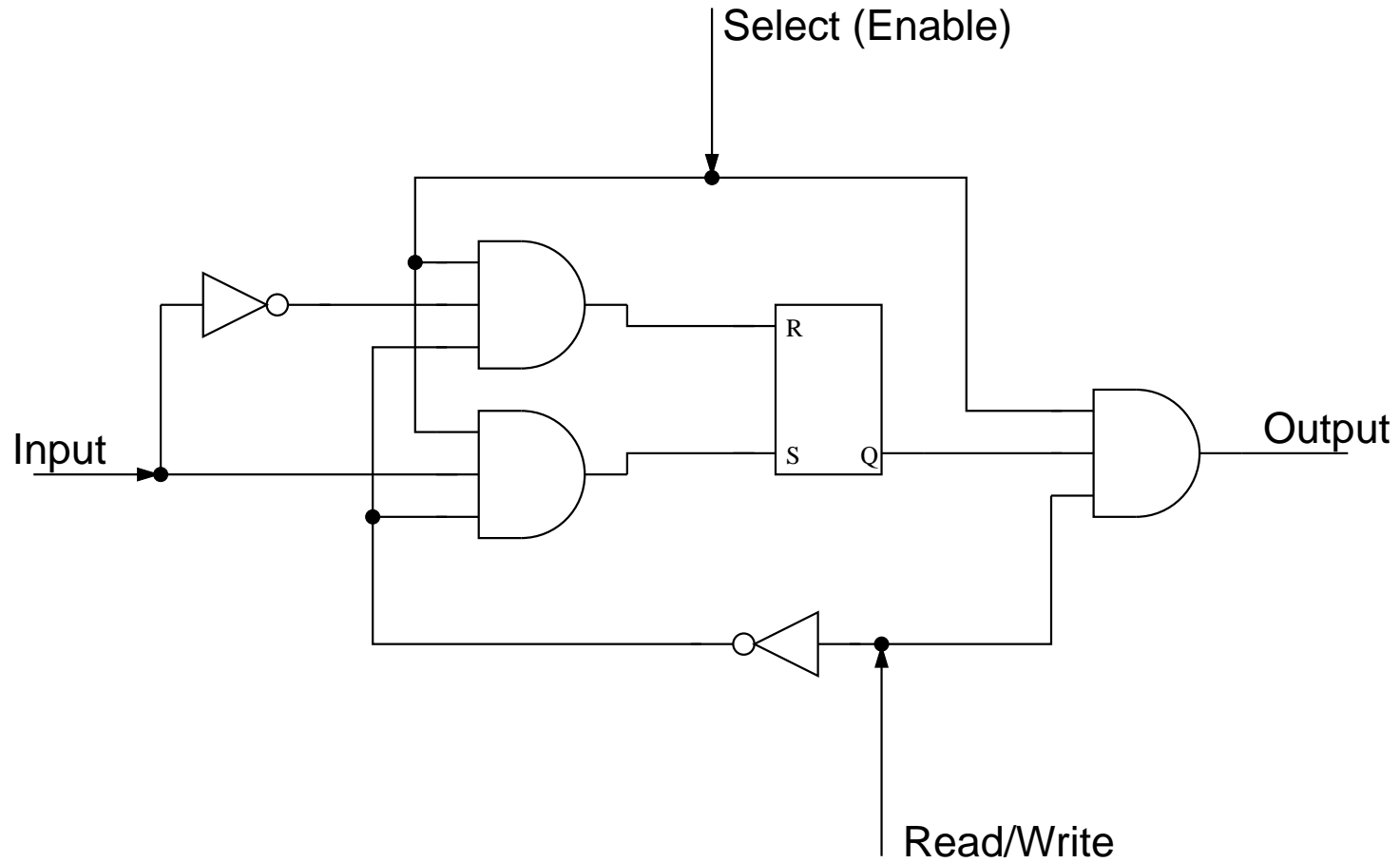
Read Cycle

1. Move the *address* of the requested word to MAR
 2. Turn the *read* input line on
 3. The content of the requested word will be transferred to MBR
- ★ Steps are done sequentially

Read Cycle



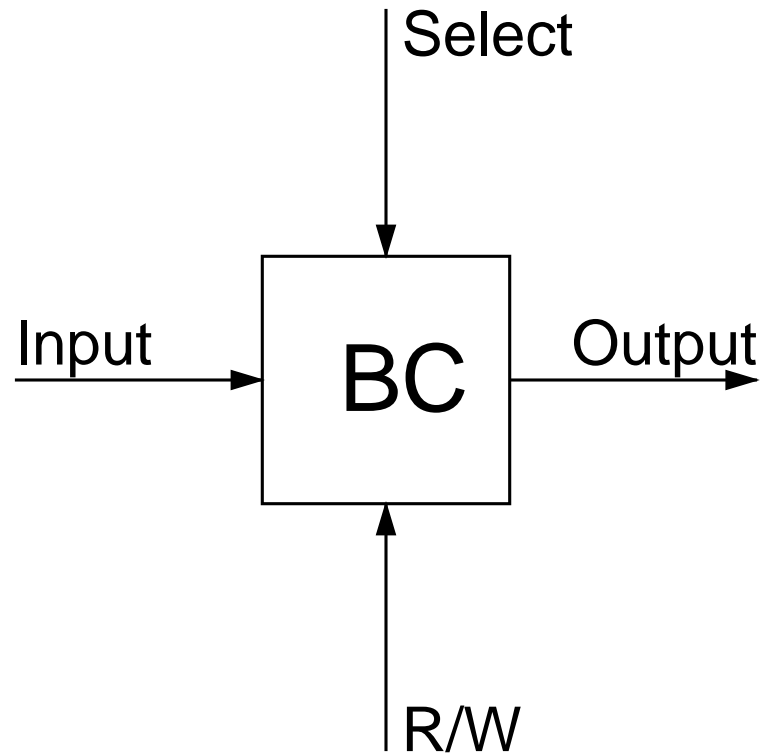
Basic Memory Cell



Basic Memory Cell - Notes

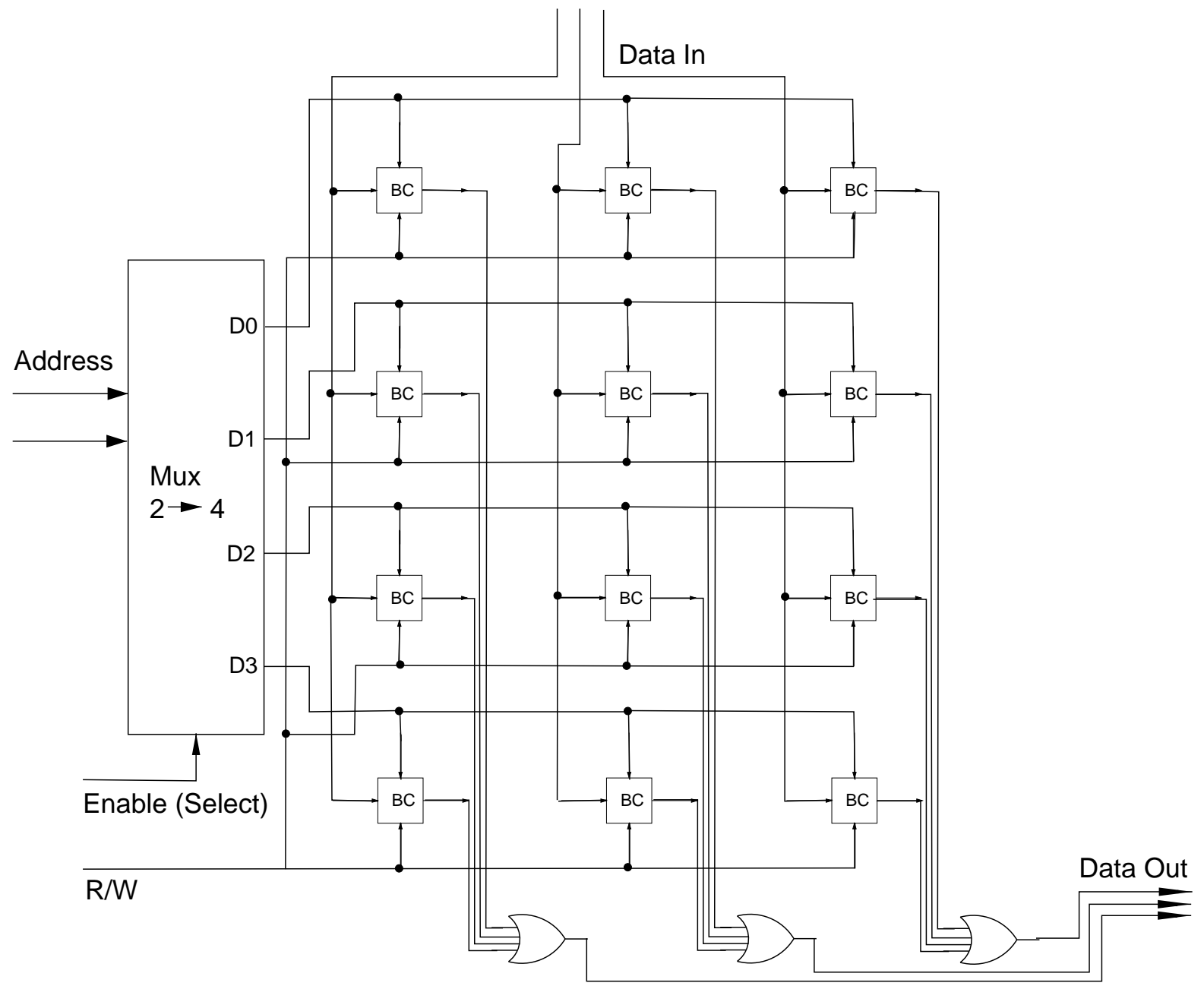
1. Uses a **latch** and not a **flip-flop** (asynchronous)
2. When not activated outputs zero
3. R/W line: read=1 write=0

Basic Memory Cell - Symbolic

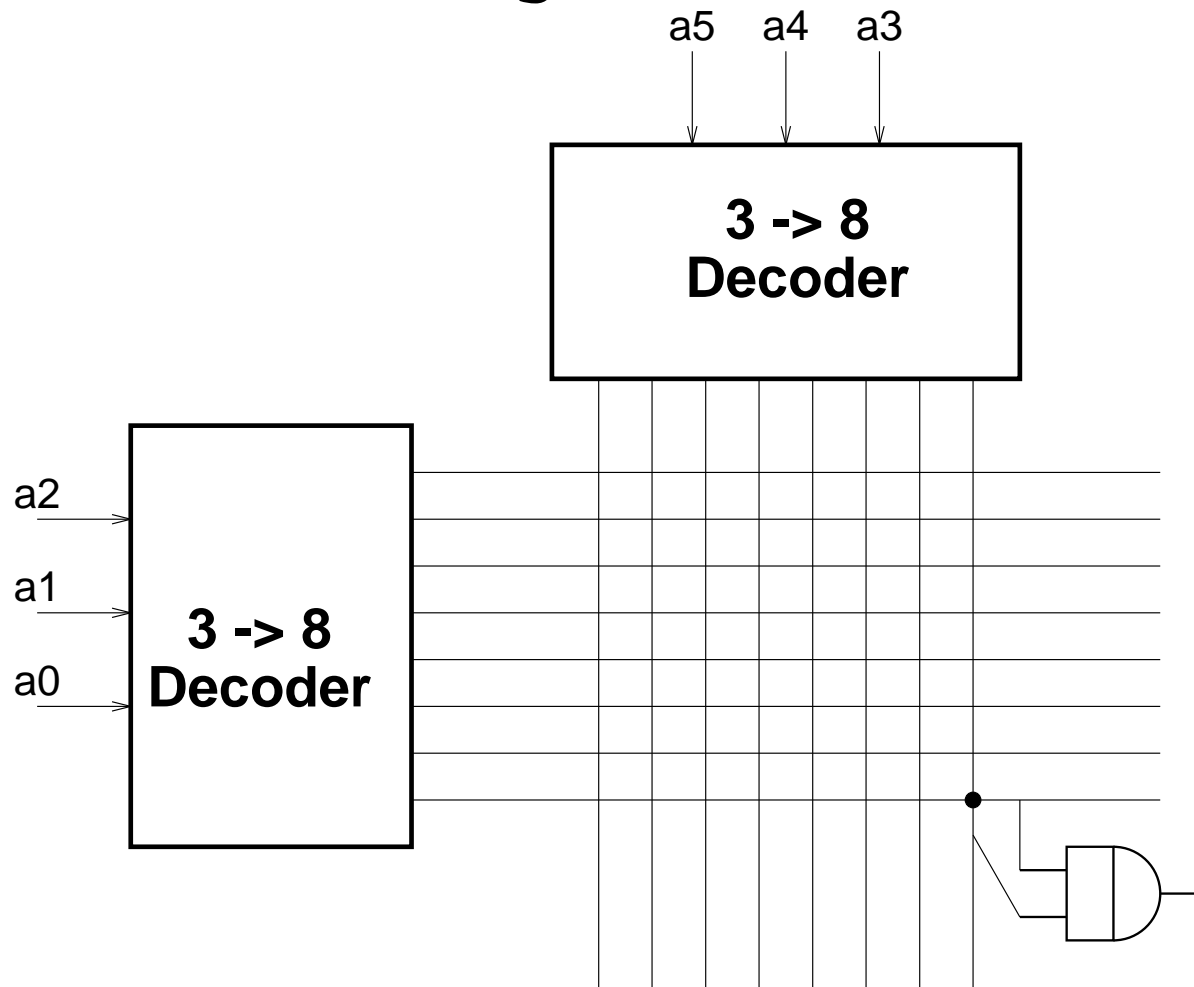


From Basic Cells to RAM

- Use decoder to translate addresses to enable signals
- Use **OR** to get a single output from the cells
- Use multiple cells with same address to increase word width



Coincident Decoding



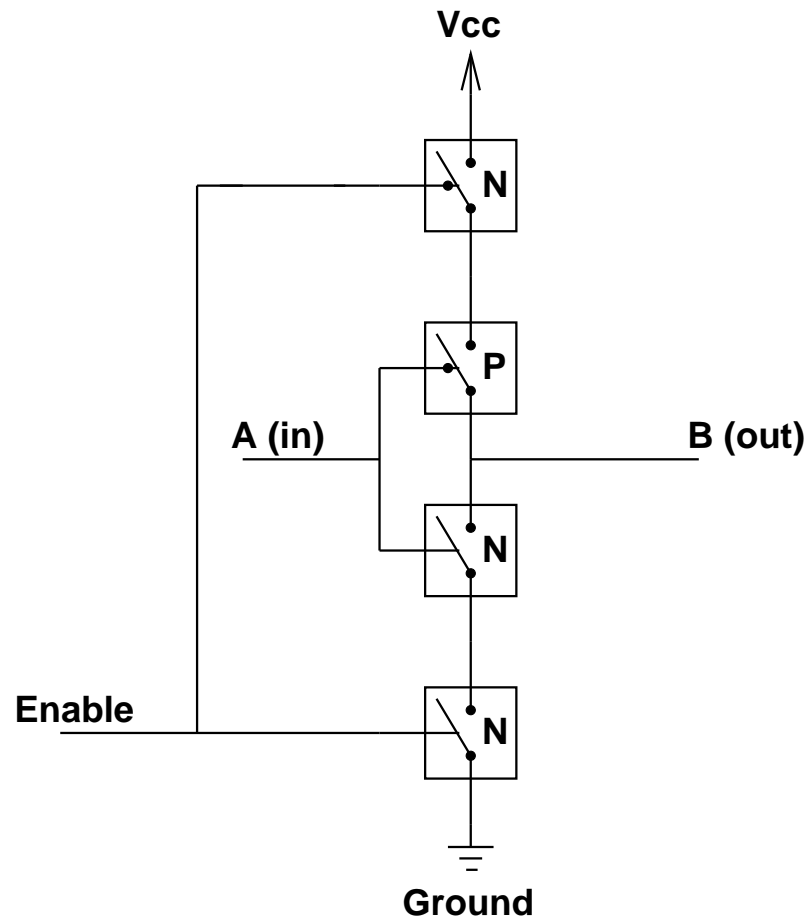
Fan-in Problem

The fan-in (number of input lines) of the **OR** gate grows exponential with the number of address lines. In fact, it is equal to the number of words in the RAM (RAM length).

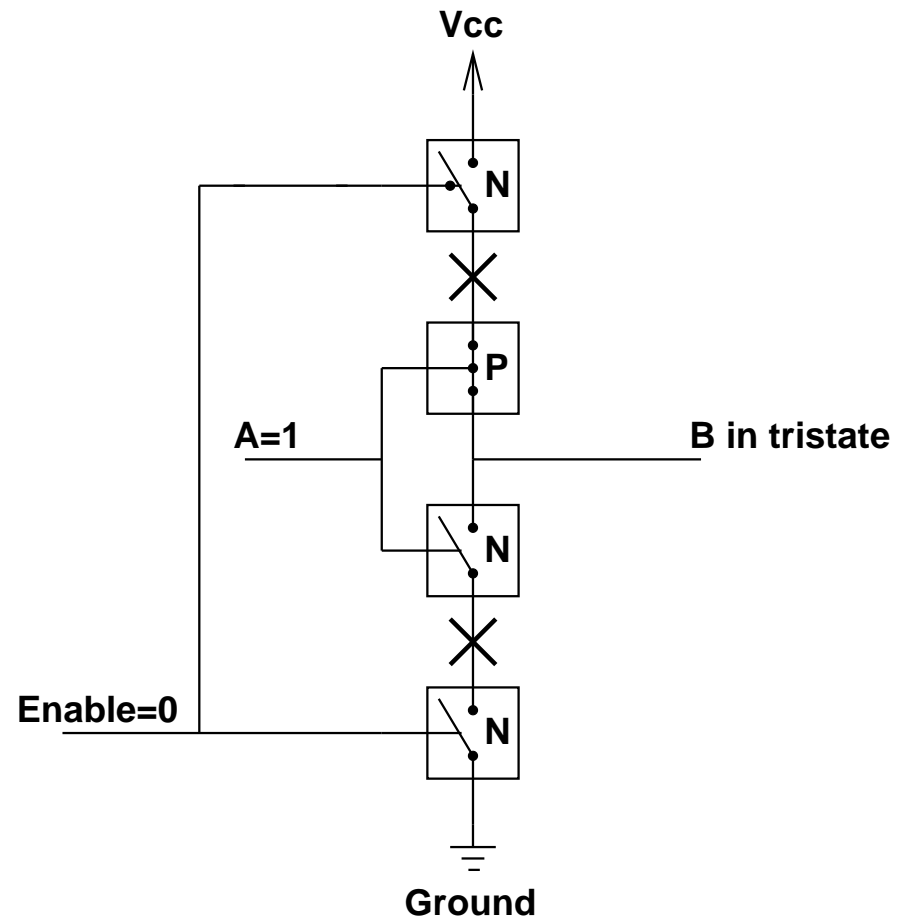
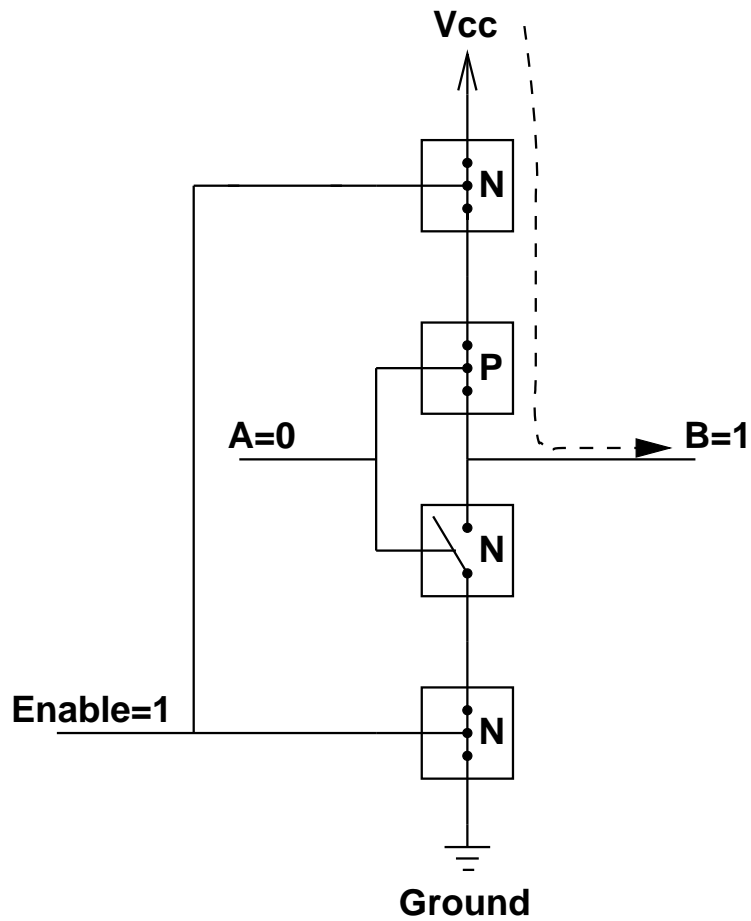
Solution:

1. Use a tree of **OR** functions (slow)
2. Use the electrical properties of digital switches: **BUS**

Three-state (tristate) Device



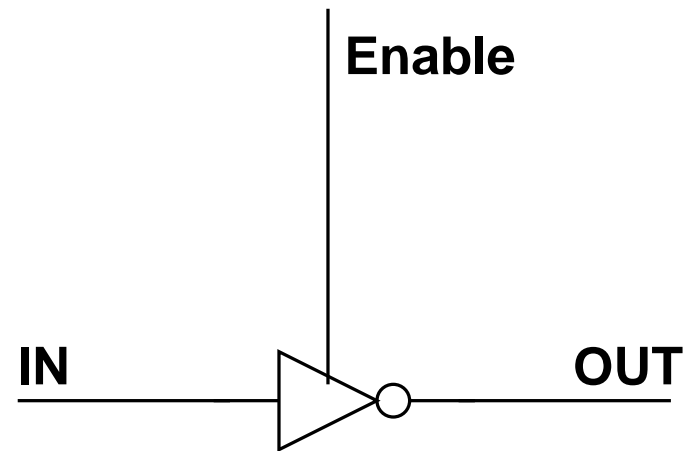
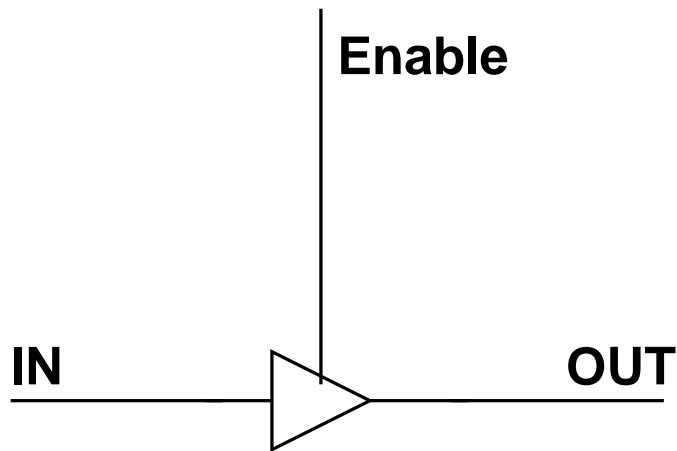
Three-state Device at Work



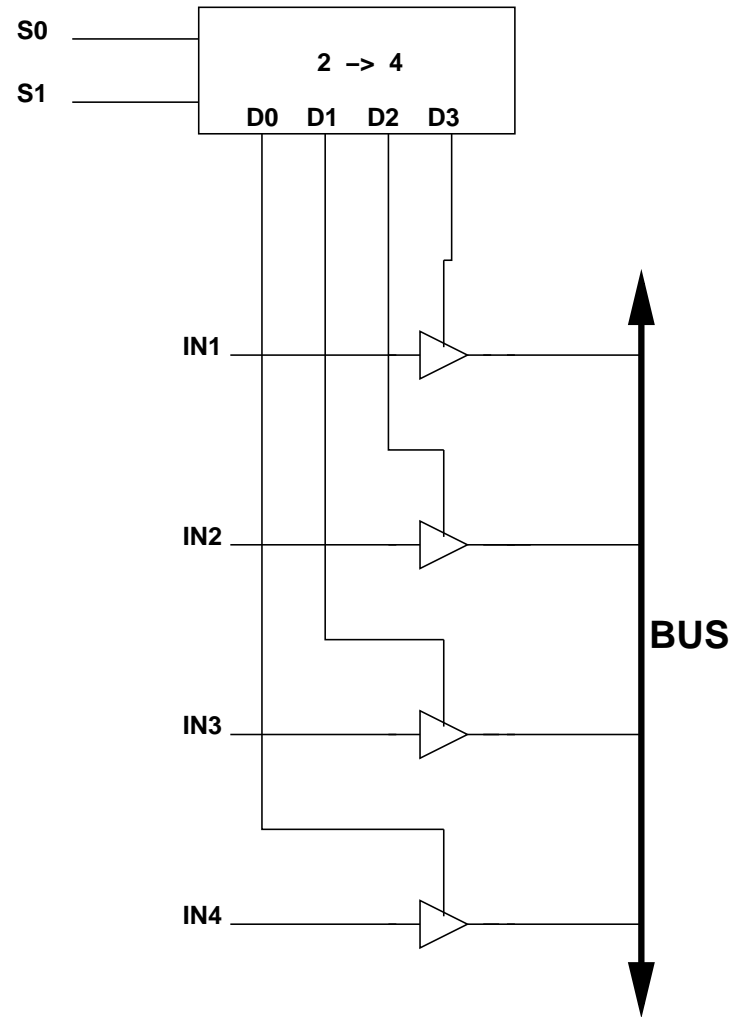
Three-state Device

When Enable=1 behaves like a **NOT/Buffer**

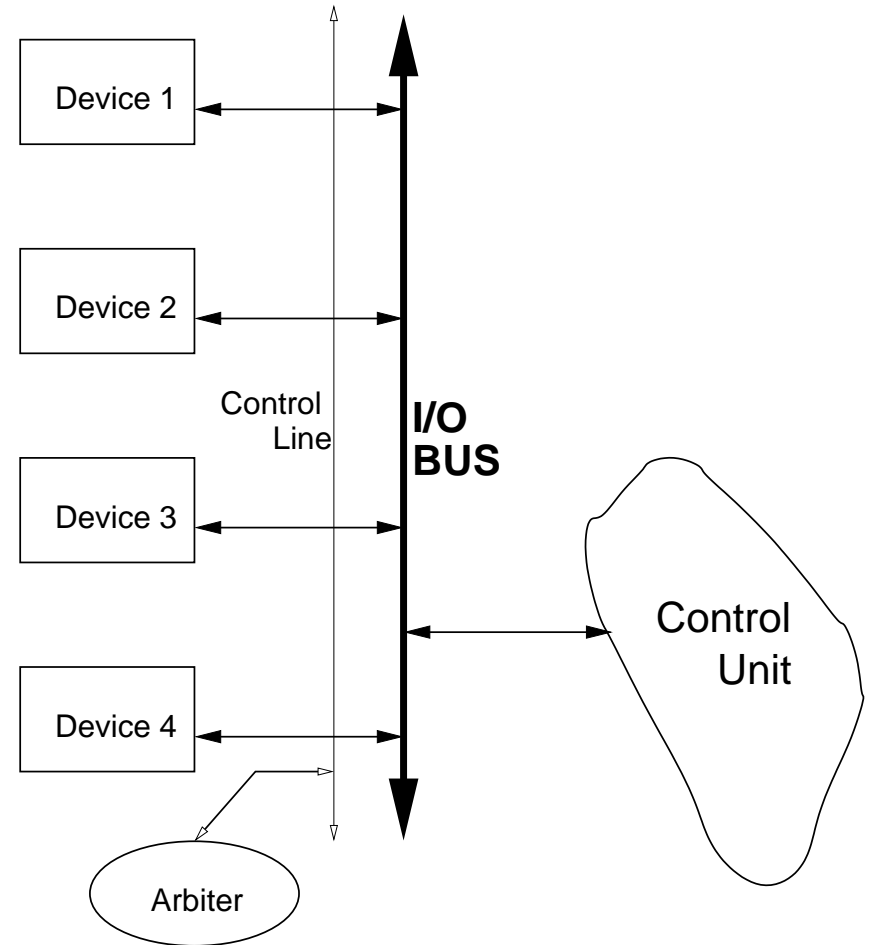
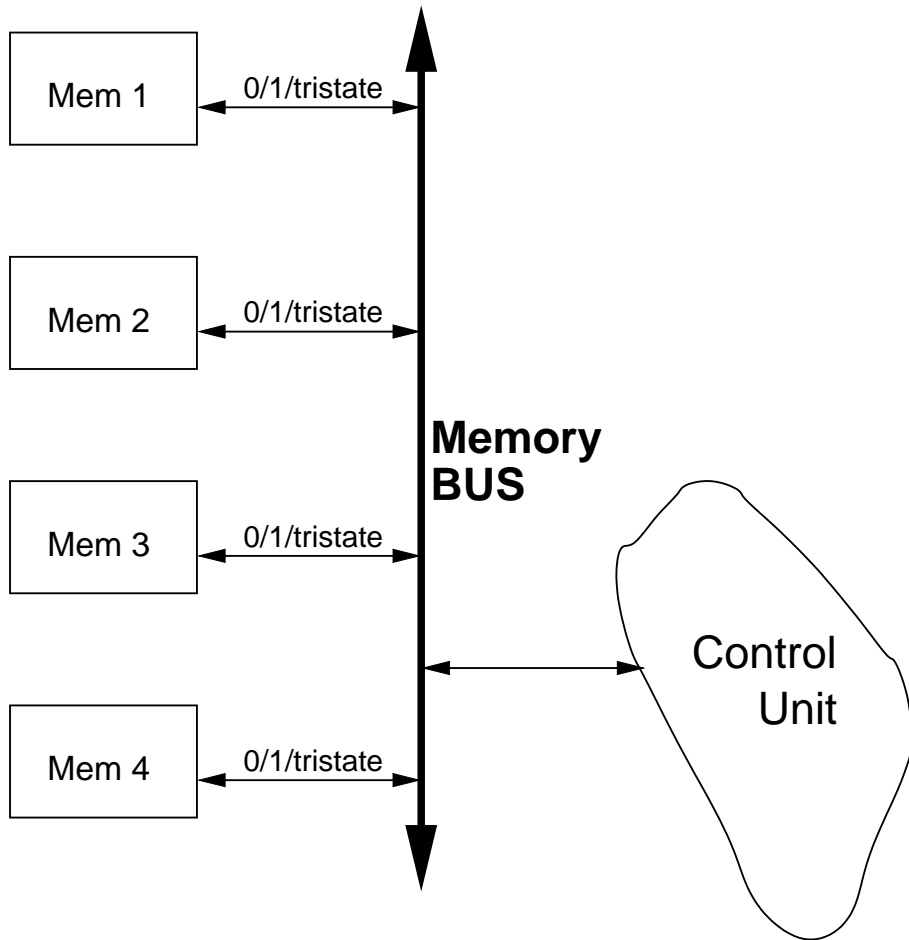
When Enable=0 **B** is disconnected from **A** (third-state)



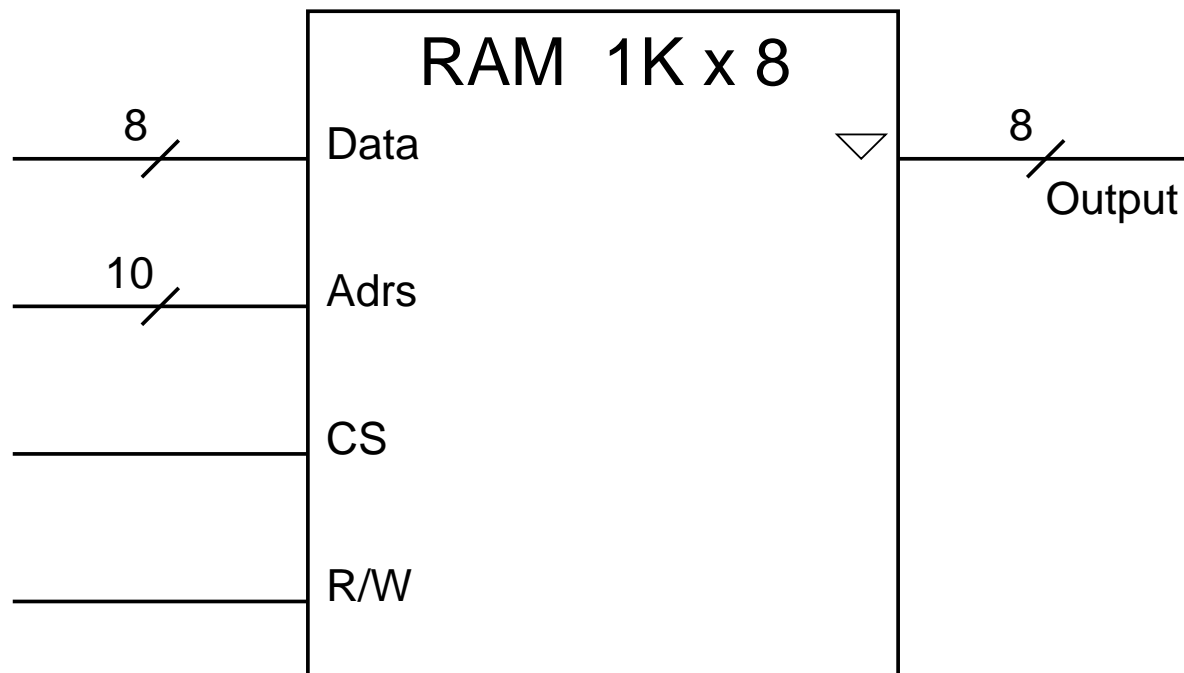
Memory BUS



General BUS Architecture

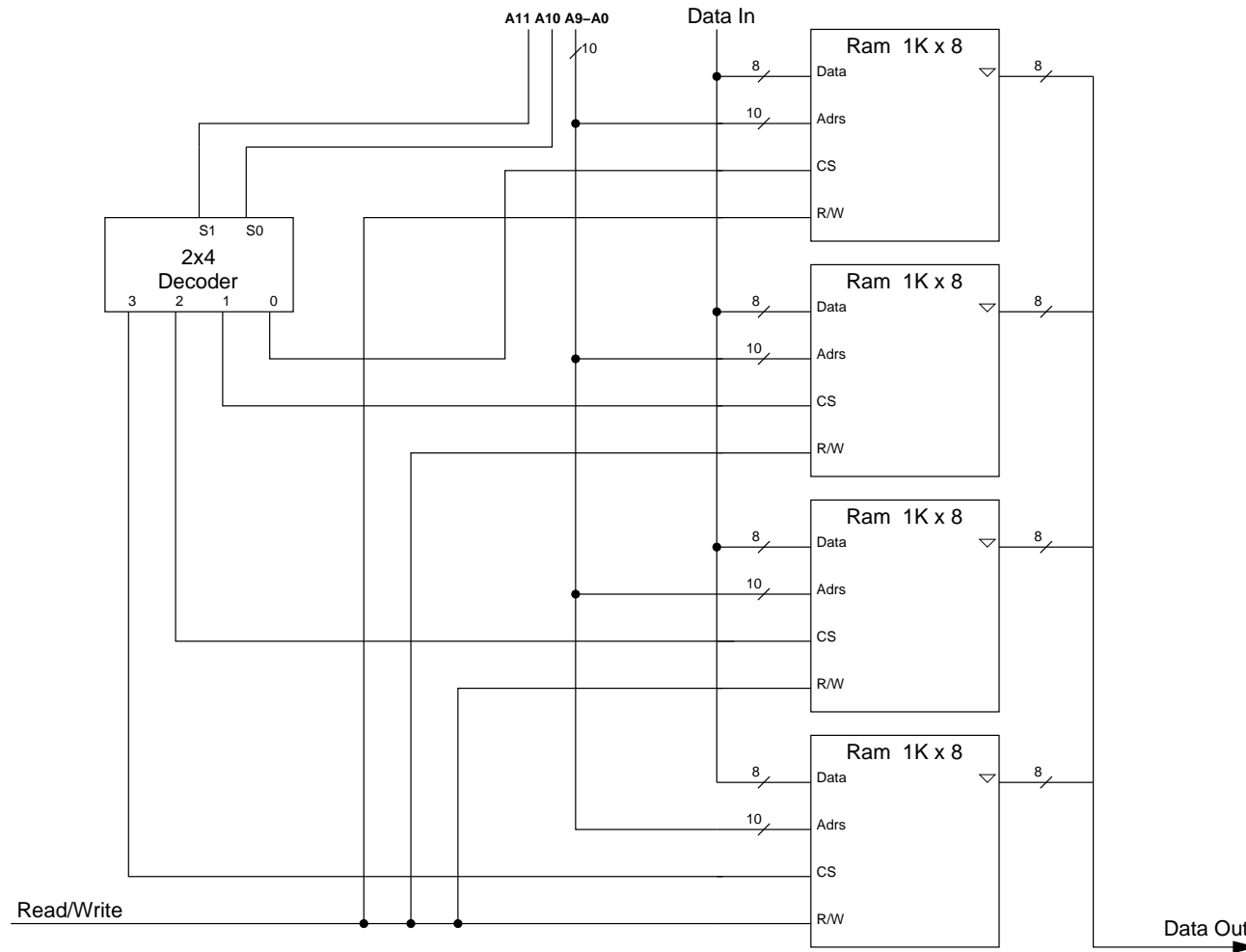


Standard RAM Chip

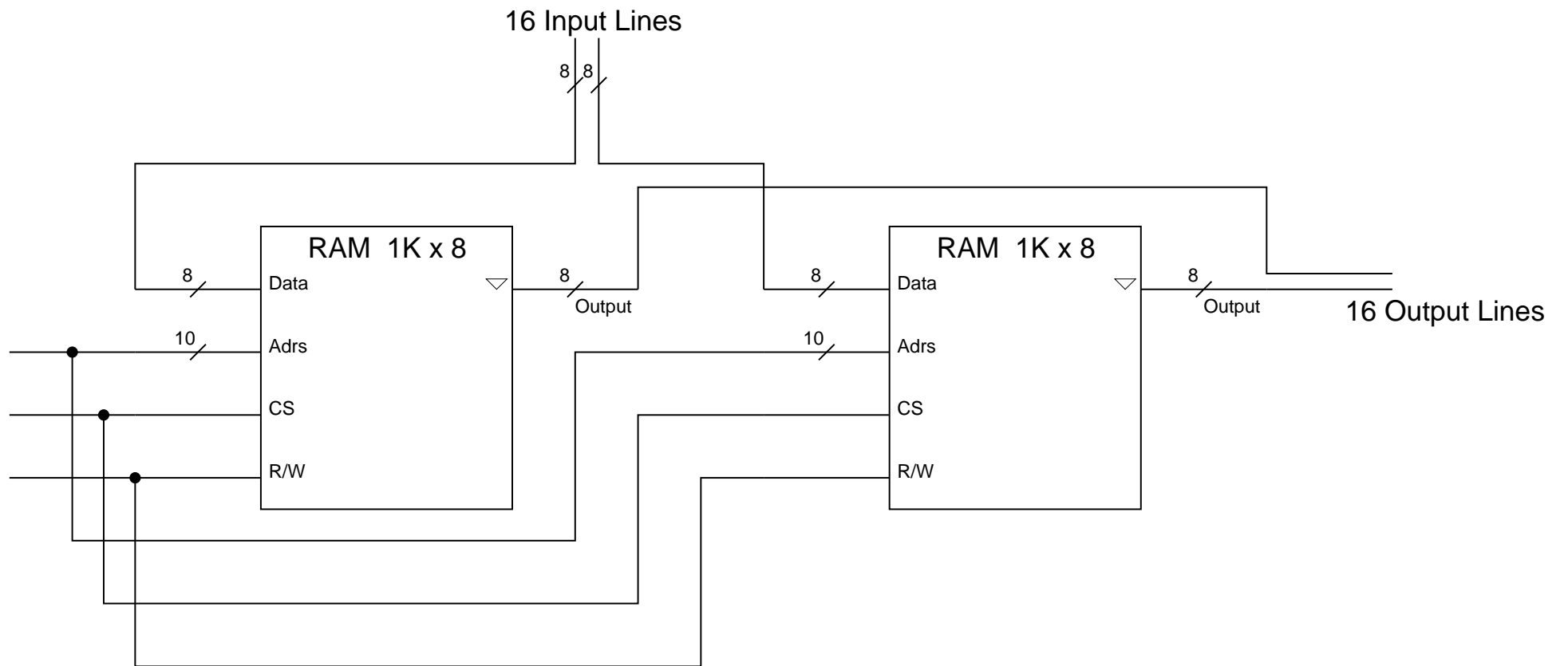


CS – Chip Select

Increasing RAM's Size



Increasing RAM's word-length



Memory Organization

- Memory viewed as large single dimensional array with address
- A memory address is an index into the array
- “Byte addressing” means that the index point to a byte (8 bits) \Rightarrow word-length is 8
- Memory buses of current CPUs have 32 lines and can read 4 bytes at a single time. This is achieved by increasing the word-length and operating RAM units in parallel.