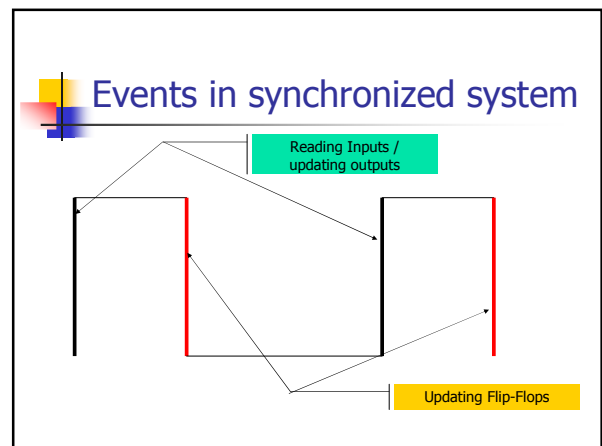


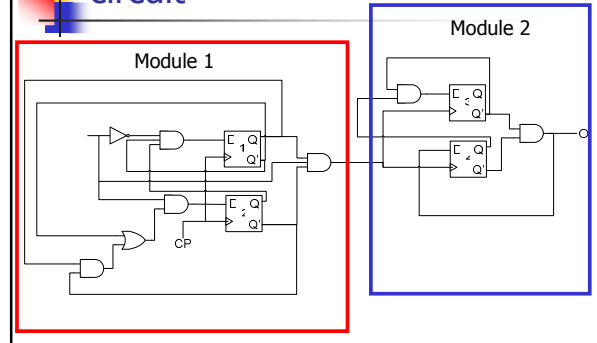
Solution to Question 2 Exercise 7



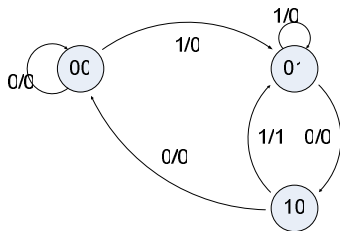
The requirements:

- All the inputs to the FF must be stable at least t_{setup} before the update of the FF
- All the outputs of the circuit must be stable on their right value, as close as possible to the updating of inputs.

Analyze the timing of the circuit



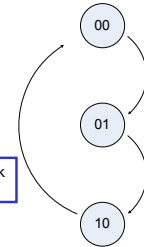
1. Analyze the state machine of module 1



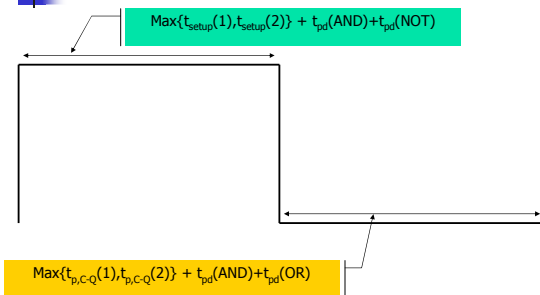
1. Analyze the state machine of module 2

Note: Module 2 is a counter. It progress each update of the FF To the next state.

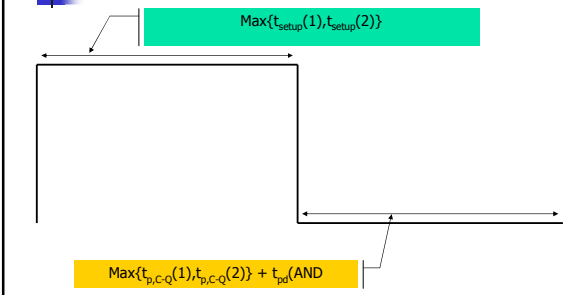
The update of the FF is when the clock Of the FF goes from 1 to 0.



Set the timing of module 1 when it is independent



Set the timing of module 2 when it is independent





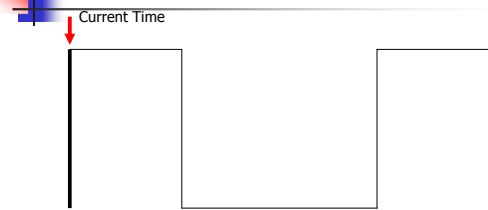
The "0" of a circuit:

The time it take the circuit output to stabilize from the negative pulse of the clock.

Examine the "Clock" of module 2.

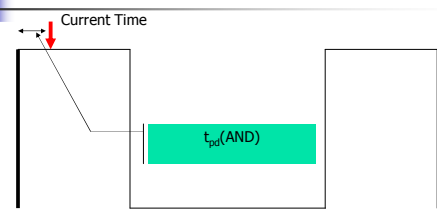
1. Suppose that module 1 is in state 10.
2. Suppose that now the input is 1

The clock of module 2



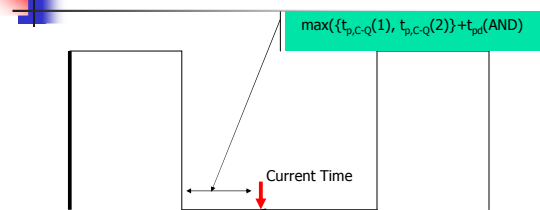
I = 1	Encounter Module = 10	Module 1 output = 0
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The clock of module 2



I = 1	Encounter Module = 10	Module 1 output = 1 The Clock of module 2
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The clock of module 2



Note, here the clock of 2 Become 0 (!).

I = 1	Encounter Module = 01	Module 1 output = 0 The Clock of module 2
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The time "0" of module 2 should be

