DFT Glossary of Terms and Abbreviations (with Definitions)

For Hebrew University of Jerusalem, School of Computer Science and Engineering, Course 67703 "DFT & JTAG Technology" Graduate Students

This glossary of terms and abbreviations reflects terms used in this course but may not reflect terms commonly used in electronics

Ad-hoc DFT - Various informal design practices, as opposed to structured or automated techniques, to increase design testability.

ATE – Automatic Test Equipment, the machines used to test PCB after fabrication.

ATPG – Automatic Test Pattern (Program) Generation (Generator). A software tool to generate test vectors algorithmically. A set of deterministic algorithms that create test vectors specifically targeting a fault selected from a set of faults. The resulting test vectors are stored externally to the CUT. ATPG is a non-embedded test technology.

At-speed Test – Testing at actual clock speeds, rather than slower external tester speeds. Refers to a variety of both memory and logic test techniques to detect timing-related defects that are only apparent when the device is run at system speeds.

BIST - Built-In Self-Test, a hierarchical DFT strategy that reduces the need for external test. Circuitry added to a design (or embedded) for the purpose of testing the design, including memory BIST and logic BIST.

Boundary-Scan - The practice of inserting a ring of scan (control, observe) cells around a chip's I/O pins and control port for the purpose of board level test access, standardized by IEEE 1149.1.

Boundary-Scan Register (BSR) – A serial shift register of Boundary-Scan cells that is used to observe and control the pins of a chip.

BS – Boundary-Scan

BSDL – Boundary-Scan Design Language. a subset of VHDL, the standard description language for Boundary-Scan devices that comply with the IEEE 1149.1 Std.

Bus contention – Two bus drivers simultaneously active and in opposite states.

Capture – A Boundary-Scan operation at which data present on an input signal line is loaded into a memory element of the BSR.

Clock Skew – The delay difference in the delivery of a clock edge to elements at different locations on the clock distribution network.

Combinational Logic – Logic that does not contain any flip-flops (F/F) latches, or memory components.

Controllability - The ability to set internal nets, nodes, device inputs or outputs to a known logic states.

Core Logic – The functional logic performing the wanted non-test functions.

CUT - Circuit Under Test. Refers to the device that is currently being tested (sometimes DUT, for Device Under Test).

Defect – A physical problem in PCB or device manufacturing.

DFT - Design-for-Test. The discipline uniting design and test aimed to increase design testability and made the design easier to test. DFT also provide access (controllability and observability) to otherwise hidden internal states of the circuit.

DR – Test Data Register.

DRAM – Dynamic Random Access Memory, a memory that uses a capacitor as a storage element and requires the application of power and a "refresh" event to retain its data.

DUT - Device Under Test. Refers to the device that is currently being tested.

Failure - A test vector response that is measured at the tester and compared to the predicted "expected response" and does not match.

Fault Masking - A fault that is not able to be detected due to a circuit configuration problem such as reconvergent fan-out or redundancy.

Fault Model - A mathematical model of faulty behavior that can be used to access the compliance of a circuit to various criteria. For ex., structural compliance can be verified by using a fault based on a stuck-at fault model, timing compliance can be verified by using a fault based on a delay fault model, etc.

Fault Coverage - A testability measure determined by the percentage of faults detected by a pattern set divided by all possible faults in the design.

Fault Simulation - The process of simulating a pattern set in the presence of faults to determine fault coverage for a design.

Functional Test – A test process that checks some aspect of the expected design behaviour, for ex. performance at-speed. Functional testing verifies the input-to-output behavior of the circuit.

Good Circuit (Known Good Board, KGB) - A circuit description or real PCB without any faults used as the comparison standard against which the faulty circuit is evaluated.

ICT Test Technique – In-circuit testing that uses a fixture containing a bad-of-nails to access individual devices on the board. Contact is made through test pads laid into the copper interconnect or other convenient contact points. Fundamentally, the ICT technique relies on physical access to devices on the board.

IEEE 1149.1 – Boundary-Scan standard formed by JTAG, the IEEE 1149.1 standard committee.

Instruction Register (IR) – The IR selects the test to perform and/or the test data register to access, and also allows shifting out of the status information.

Interconnect Test – A test for the correctness of all PCB level interconnects.

JTAG - Joint Test Action Group, the group that began the Boundary-Scan IEEE 1149.1 standard. It is now commonly used in slang form as a synonym for 1149 set of standards.

Least Significant Bit (LSB) – The lowest order or the right-most bit of a register (corresponds to bit number 0)

Net – Configuration of connected-through copper tracks/wires on a PCB. An implicit or explicit descriptor for a connection in a netlist.

Netlist – A text-based design description that represents the schematic of the circuit.

Observability - The ability to observe values from internal nodes of the design after they have been driven to a known logic state.

Open – A name of a fault caused by an interrupted electrical connection, for ex. between a component pin and the PCB track or caused by a broken copper track.

Parametric Testing – A form of testing where the voltages, currents, and timing are measured for compliance against specified values.

Path Sensitization – The establishing of a propagation pathway (D-algorithm) from one point in a circuit to another one to propagate a fault effect to an observe point. This analysis is done by an ATPG tool during the generation of vectors.

Pattern – A grouping of individual (test) vectors.

PCB – Printed Circuit Board

PI – Primary Input, an input signal that is directly controllable by an ATPG tool during test vector generation.

PO – Primary Output, an output signal that is directly observable by an ATPG tool during test vector generation.

RAM – Random-Access Memory, a type of semiconductor memory that stores digital information temporarily and can be changed as required.

Redundant Fault – A fault that cannot be detected with a test vector.

Scan Chain - A connection of sequential elements converted into a shift register, which aids testing by shifting in test data, capturing system data and shifting out system responses.

Scan-DR – TAP controller state that applies the scanning process to each test data register, comprises some individual controller states as Capture-DR, Shift-DR, Exit1-DR, Pause-DR, Exit2-DR, and Update-DR.

Scan-IR – TAP controller state that applies the scanning process to the instruction register, comprises some individual controller states as Capture-IR, Shift-IR, Exit1-IR, Pause-IR, Exit2-IR, and Update-IR.

Serial Vector Format (SVF) – A board level test pattern format used with IEEE 1149.1 board level software.

Shift – A Boundary-Scan operation of a serial shift register (e.g. BSR) at which data is shifted through the serial path.

Short – A name of a fault caused by an electrical connection between two or more signal pins or copper tracks/wires on a PCB.

Stuck-at – A name for a fault that causes a PCB signal connection to be fixed at logical level '1' or '0', independent of the driving signals.

Structural Test – A test process based on a pattern set that has a known defect or fault coverage.

TAP - Test Access Port. The standard test pins used for IEEE 1149.1, including TCK, TMS, TDI, TDO and optional /TRST.

TCK – Dedicated Test Clock. This mandatory terminal of the TAP is driven by the clock that controls the synchronous operation of the TAP.

TDI – Test Data-In. Serial test data shifted in with a default value of 1. A mandatory terminal of the TAP.

TDO – Test Data-Out. Serial test data shifted out with a default value of Z. This mandatory terminal of the TAP is only active during the shift operation.

Testability - A measure of a design's controllability and observability.

Test Coverage - A testability measure determined by the percentage of faults detected by a pattern set divided by all testable faults in the design.

Test Vectors – The logic 1s and 0s applied to a PCB specifically for the test process.

TMS – Test Mode Select. Serial input control signal with a default value of 1. A mandatory terminal of the TAP.

TRST – Test Reset. Asynchronous TAP controller reset with a default value of 0, the optional terminal of the TAP.

Undetected Faults – Faults that are not exercised or observed by the applied set of test vectors.

Update – A defined operation of a serial shift register element (e.g. Boundary-Scan cell) at which the content of the scan cell is transferred to an output element.

Virtual Access – As opposed to physical access, a term used to indicate that Boundary-Scan cells can be used to access board connections and through these connections the inputs and outputs of non-BS devices (clusters).

Walking Sequence – A sequence of test patterns at which the test vectors contain only one '1' between all zeros (walking '1') or vice versa (walking '0'). This vector shifts through the scan path such that the logical value, either the '1' or the '0', is applied to all nets, one at a time.